

the specified traffic pattern, 20000 packets were injected in the network where k . Each packet has 5 flits. Owing to E_{link} and E_{router} values are similar for all technology nodes presented, the energy consumption of different mesh NoC sizes operating in 1 GHz is shown in figure 6 considering MOS routers NoCs and nanoelectronic routers NoCs. As can be seen, the router consumes the most part of the energy in a communication architecture, since the in both cases copper interconnects were used. In this way, using nanoelectronic devices is a promising alternative for reducing the total energy consumption.

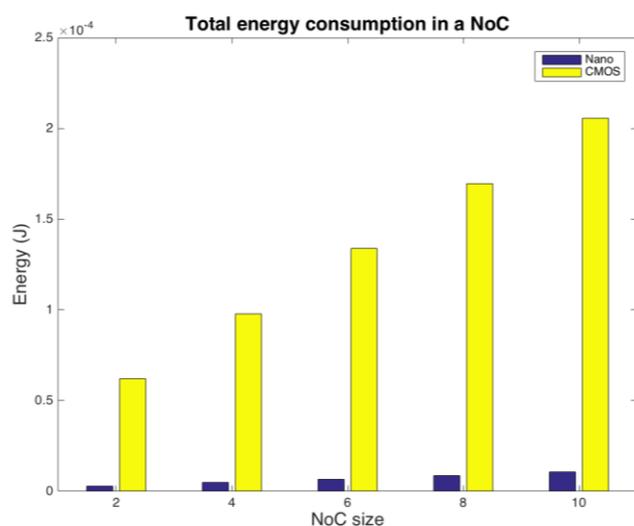


Figure 6. Performance comparison between MOS and nanoelectronic NoCs

5 Conclusions

In this work, the performance evaluation of a NoC interconnected architecture using nanoelectronic devices was proposed and its energy was estimated. This work shows the potential of using nanoelectronic devices for NoC architectures. With the reduce of the devices, the energy dissipated in a system is becoming a huge problem. Thereby, the gain introduced by nanodevices is very promising and can provide a substantial reduction in the total energy of the system.

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References:

[1] J.A. Davis, R. Venkatesan, A. Kaloyeros, M. Bylansky, S.J. Souri, K. Banerjee, K.C. Saraswat, A. Rahman, R. Reif, and J.D. Meindl, "Interconnect Limits on Gigascale Integration

(GSI) in the 21st Century," Proceedings of the IEEE, vol. 89, no. 3, pp. 305-324, March 2001.

- [2] J. G. Guimarães and J. C. da Costa, "Interconnect Impact on the Performance of a SET-Based Network-On-Chip Memory Circuit" 14th IEEE International Conference on Nanotechnology, 2014, Toronto, vol. 1, pp. 287-290.
- [3] M. M. Wanjari, P. Agrawal and R. V. Kshirsagar, "Design of NoC Router Architecture using VHDL", International Journal of Computer Applications 115(4), pp.18-21, April 2015.
- [4] C. A. Nicopoulos, "Network-on-chip architectures: a holistic design exploration", Ph.D. Thesis, Department of Electrical Engineering, Pennsylvania State University, 2007.
- [5] S. Park, M. Qazi, L.S. Peh and A.P. Chandrakasan, "40.4 fJ/bit/mm low-swing on-chip signaling with self-resetting logic repeaters embedded within a mesh NoC in 45 nm SOI CMOS", Proceedings of Design Automation and Test in Europe (DATE), March 18–22, Grenoble, France, 2013.
- [6] M. O. Telles and J. G. Guimarães, "Single-electron shift register", Microelectronics Journal, vol.44, 332 (2013).
- [7] G. Lientschnig, I. Weymann, P. Hadley, "Simulating hybrid circuits of single-electron transistors and field-effect transistors", Jpn J. Appl. Phys., vol. 42, no. 10, pp. 6467-6472 (2003)
- [8] Linear Technology – Design Simulation and Device Models Retrieved, December, 2015, from <http://www.linear.com/designtools/software>
- [9] N. Srivastava, H. Li, F. Kreupl, K. Banerjee, "On the applicability of single-walled carbon nanotubes as VLSI interconnects", IEEE Transactions on Nanotechnology, vol. 8, no. 4, pp. 542-558
- [10] C. Thiruvankatesan, J. Raja, "Studies on the application of carbon nanotube as interconnects for nanometric VLSI circuits", ICETET'09, pp. 162-167.
- [11] B. O. Câmara, J. G. Guimarães and J. C. da Costa, "Proposal of a router circuit based on nanoelectronic devices" TechConnect Briefs 2016 - Advanced Manufacturing, Electronics and Microsystems, 2016, Washington, vol. 1, pp. 183 – 187, May 2016
- [12] G. B. Bezerra, "Energy consumption in networks on chip: efficiency and scaling", PhD Theses, The University of New Mexico, 2012.