A TG based 2-Stage High Frequency Rectifier with Current Booster Designed Using 45nm CMOS process for Low Power RF Energy Harvesting Application

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Abstract: - As the 5G communication technology is becoming a reality, the importance of energy harvesting to provide self-sustainability to the communication network is gaining more importance with reliable and faster data transfer capabilities. So, as achieving self-sustainability in terms of power is a significant goal, hence designing an energy harvesting system is an important aspect. The primary element of the energy harvesting system is the high frequency rectifier. But designing a rectifier at high frequency is very crucial. The main bottleneck of such a design is offered by the leakage in the CMOS device which in turn limits the percentage conversation efficiency (PCE) to be achieved at lower signal power. Also achieving a acceptable voltage and current at the output is essential. This paper presents a two stage high frequency rectifier design based on transmission gate (TG) with a current boosting mechanism for RF applications. This design achieves a maximum PCE to 90% at -2dBm in a double stage realization. This result is observed to be the highest efficiency in its class as compared to recently reported works. It performs well over a wide band of frequencies and is capable of working in commercially relevant frequency bands for mobile communication which is clearly depicted by the frequency response. Also this circuit uses optimal number of devices with total dynamic power dissipation of 4.6 μW.

Key-Words: - Energy Harvesting, Power Conversion Efficiency, Transmission Gate, CMOS, Current Booster, Radio Frequency (RF)

1 Introduction

With the advent of 5G communication, energy conservation and management is attaining more attention apart from the technological requirements of faster and reliable communication. Hence self-sustainability in all wireless networks is becoming an issue of potential importance. To address self-sustainability as well as virtual operation energy harvesting capability must be embedded into the network. As the energy harvesting capability of a network makes the life-time of the network augmented, it facilitates the installing of a network at any remote location and eliminates the requirement of an electrical power source. Hence energy harvesting is becoming an indispensable element in communications, medical as well as surveillance applications in the near future.[1][2]. Several natural and artificial sources can be well utilized for harvesting energy. As the nature of the sources are diversified and as there is a requirement to transfer the harvested energy from node to node, harvesting design has to be of different capabilities and efficiencies [3].

Design of a rectifier or charge pump is the core of the energy harvester design. There are different challenges in a rectifier designs. Some of them are high frequency compatibility, low power consumption, low area in silicon substrate etc. But to maximize the power conversion efficiency (PCE), the most important criteria which the designer must address to formulate an efficient design. Cross coupled bridge configuration with differential RF input can be designed which give low on state current and small leakage current and thereby offering better PCE[4]. Voltage doubler Ultra High Frequency (UHF) rectification unit is also designed with the technique of internal cancellation to achieve a zero-threshold transistor and thereby an accepted PCE is achieved with reduced area [5]. Dickson charge pump is one of the most widely used structure for this purpose and different modifications have been presented by several designers for specific applications and efficiencies. The Dickson charge pump has been modified to reduce the leakage current with linear regulator and thereby total power consumption can be reduced [6]. Rectifier based on improved Dickson charge pump

in two configurations is presented which works in GSM band with a satisfactory PCE [7]. Also dynamic threshold reduction technique based CMOS rectifier has been designed with the use of a clamper to reduce the effective threshold voltage and increase the sensitivity and hence achieving a high PCE [8].

Several related works are reported from [9] to [18]. A relevant concept of energy harvesting for passive UHF radio frequency identification (RFID) which relies on the exploitation of the power carried by the third harmonic signal generated by the RFID chip is introduced in [9]. A load modulated rectifier with ultra low power management unit is reported in [10]. Paper [11] introduces a battery-less RF harvesting application. Two different designs of low power passive RF ID tag is presented in [12] and [13]. Paper [14] and [15] presents two CMOS based rectifier design for energy harvesting applications.

This paper presents the design of a 2-stage high frequency rectifier based on transmission gate with current boosting mechanism using the 45nm CMOS process for RF energy harvesting applications. It achieves a maximum PCE of 90% at -2dBm. This is observed to be the highest in-class PCE achieved with the use of optimum number of transistors and a significantly lower power dynamic power of 4.6μW. The attribute of the proposed design is its current boost capability, high PCE, temperature stability and wideband frequency response.

The remaining of the paper is organised as follows. Section 2 briefly explains the proposed RF energy harvesting system, section 3 deals with simulation results, comparative analysis and discussion and section 4 includes the concluding research summary.

2 Proposed 2-stage TG Dickson Rectifier with current booster

The generic RF energy harvesting system is constituted with three basic units. These are matching network, a high frequency rectifier and a power management unit. We have added a current booster network with the rectifier to have a acceptable level of current and thereby contributing towards the achievement of a significant increase in the PCE. This is shown in Fig. 1. It is evident that the matching network basically facilitates the maximum power transfer from the antenna to the rectification unit placed after this network.

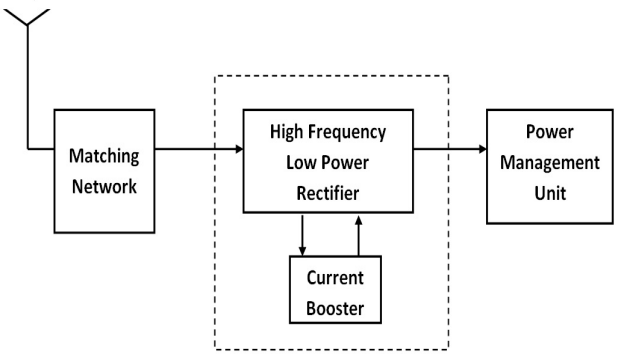

Figure. 1: Proposed System diagram of RF energy harvesting

The power generated is managed by the power management unit as per the configuration of the system and the available battery capacity. It also performs the task of distributing the excess power to the neighboring communication nodes as per the requirement. The high frequency rectifier is the core of the system and its effectiveness is determined by the PCE. The crucial design challenge lies in achieving a significantly higher PCE at lower signal power level. Also while addressing this issue the use of optimal number of devices is important to have a cost effective and practically viable solution. The concept of a transmission gate (TG) is used to design the high frequency rectifier. Also a current boosting mechanism is used to inject higher current to the device which finally contributed to the achievement of higher PCE.

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The proposed 2-stage TG based design of the Dickson rectifier with current boosting mechanism is shown in Fig. 2. It is known that the TG is a very important component for CMOS based design. As the nMOS pass transistor allows the negative voltage efficiently with less propagation time while the pMOS pass transistor permits the positive voltage to develop efficiently with less propagation time; hence transmission gate can be a viable solution for the cases where the circuit needs to deal with both positive and negative voltage levels. Also the TG is known to generate higher on state current for a wide range of input voltage.

The circuit presented in Fig. 2 is a modification done to the Dickson Charge Pump (DCP) with the use of TG and then expanding the idea to the 2-stage. The current boosting mechanism is intended to generate higher current at the output and thereby producing a higher output power. DCP is a circuit which is based on the principle of charge

multiplication. A simple DCP is configured similar to the one stage of the circuit shown in Fig.2 with two diode-connected MOSFETs and without the diode connected nMOS at the lower part of the TGs. In the negative half of the cycle the left hand side device conducts and thereby provides a charging path for the input capacitor. In the positive half of the cycle the device in the right hand side conducts and provides the discharging path to the input capacitor which ultimately facilitates the transfer of charge from the input capacitor to the output capacitor. This configuration works fine but when the circuit needs to be modelled using finer resolution technology nodes it is limited by the drain current as all the dimensions of the device. Further the supply voltage value needs to be scaled.

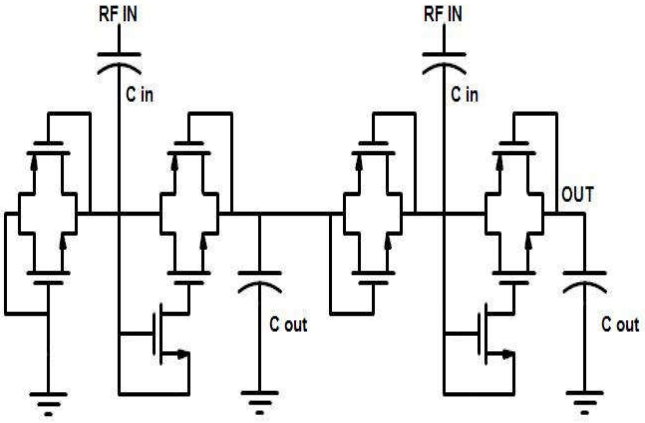

Figure 2: Proposed 2-stage TG based circuit schematic of Dickson Charge Pump

So, the output current becomes lower with scaling and the PCE also shows a decline. As TG is known for generating on state higher current and is capable of driving both the logic states successfully, hence the conventional DCP is modified with the transmission gate. Also to get a higher value of output voltage cascading of the basic unit is required. It brings the output voltage to a acceptable value. Further it has been observed that there still remains scope of enhancing the current to attain a higher PCE at lower input power. This is why a diode connected nMOS is used in between the gate and drain terminal of the nMOS part of the driver TG. It injects more current to the chain by enhancing and maintaining the gate voltage of the device.

For a negative cycle, the input capacitor will get charged by finding the path through the left side TG while in the positive cycle the charge in the input capacitor gets transferred to the output capacitor through the TG in the right side of the schematic. As the current through the TG is further made high with the use of current boosting, the output power also becomes high.

In a TG circuit when input is made positive; the pMOS will initially be at saturation and then shall switch to non-saturation state while the nMOS will be in saturation state. If we consider the I_{Dn} and I_{Dp} be the current through the nMOS and the pMOS respectively and V(t) be the RF signal voltage, then the total output current is

$$I_{out} = I_{Dn} + I_{Dp} \quad (1)$$

Again, initially

$$I_{Dp} = \beta_p/2\ [V(t) - |V_{Tp}|\ ] \quad (2)$$

But as the output voltage rises

$$I_{Dp} = \beta_p/2\ [2(V(t)-|\ V_{Tp}\ |)(V(t)-V_{out}) - (V(t)-V_{out})^2] \quad (3)$$

Also the on state current of nMOS is

$$I_{Dn} = \beta_n/2\ [V(t) - V_{out} - V_{Tn}\ ] \quad (4)$$

So the output power is

$$P_{out} = V_{out}\ .\ I_{out} = V_{out}(I_{Dn} + I_{Dp}) \quad (5)$$

The power conversion efficiency (PCE) can be calculated as

$$PCE = (P_{out} / P_{in})*100\% \quad (6)$$

The P_{out} with a normal configuration would have been either V_{out} (I_{Dn}) or V_{out} (I_{Dp}). So the P_{out} would have lower and thus yielding a low PCE. So better PCE can be attained with TG based configuration. Also with the current booster I_{Dn} rises, making further enhancement of the PCE.

3 Results and Discussion

The designed circuit is simulated and we discuss the results obtained in following Sub sections. By using the optimization techniques as reported in [16][17] the aspect ratio of both the nMOS and the pMOS is tailored as follows

L_n	W_n	L_p	W_p
45nm	150nm	65nm	150nm

Table 1: Aspect Ratios of both nMOS and pMOS devices

Where Ln and Lp are the channel length of the nMOS and the respectively and Wn and Wp are the channel with of the nMOS and pMOS respectively.

3.1 Design Simulation

The simulation of the transient response of the designed circuit is performed. The DC output voltage with time for different value of input capacitances is presented in Fig. 3. The output voltage shows a dependence on the value of output

capacitance as well as input capacitance. The DC output voltage with time for different value of output capacitances is presented in Fig. 4.

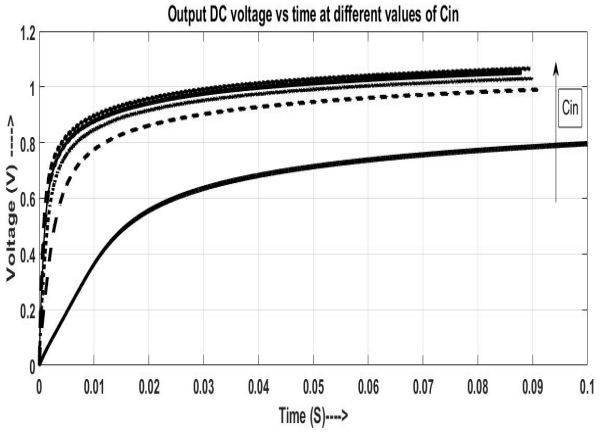

Figure 3: Output DC voltage for different value of input capacitances

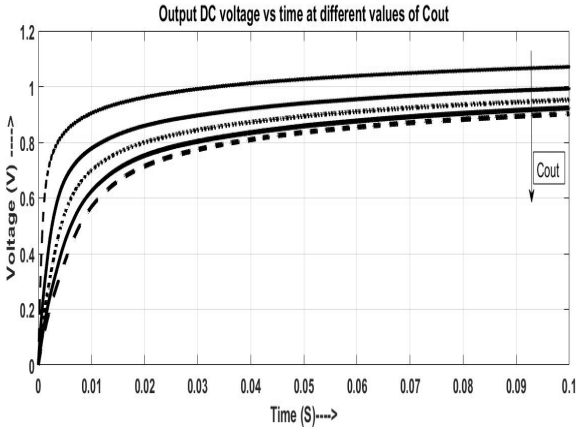

Figure 4: Output DC voltage for different value of output capacitances

The variation in the output voltage and current with the variation in the intput capacitance is shown in Fig. 5. It is observed that both the output DC voltage and current shows an increase with the increase in the capacitance value.

The output has a dependence on the output capacitance too. It is shown in Fig. 6. It depicts that with the increase in the value of C_{out} the voltage value decreases but the current shows an increase.

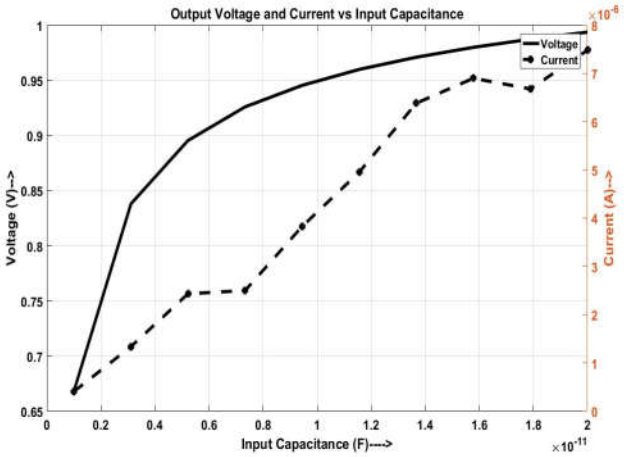

Figure 5: Output voltage and current vs input capacitance (C_{in})

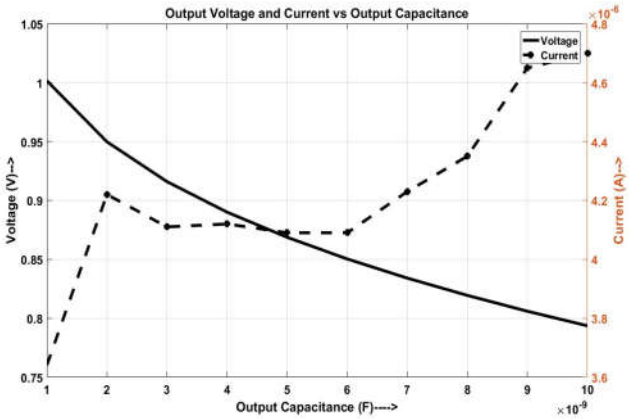

Figure 6: Output voltage and current vs Output Capacitance (C_{out})

For better performances the value of capacitance required can be estimated Also the dependence of the output with device dimensions are investigated.

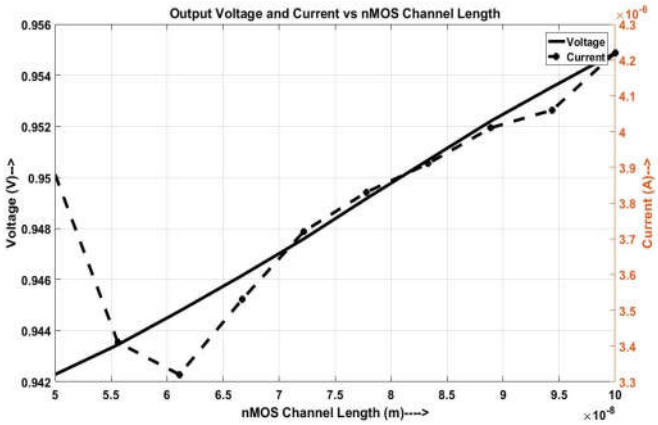

Figure 7: Output voltage and current vs nMOS channel length (L_n)

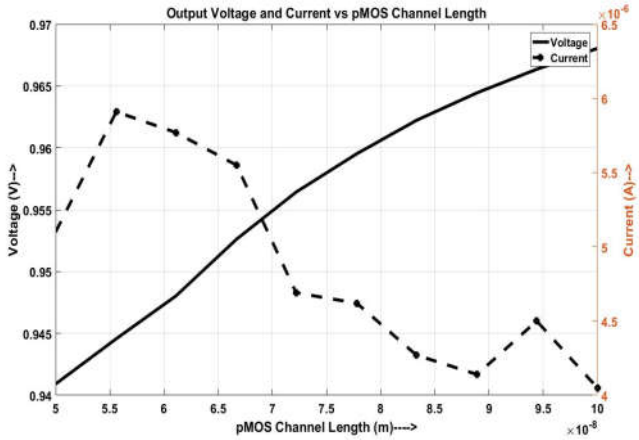

Figure 8: Output voltage and current vs pMOS channel length (L_p)

Figs. 7 and 8 represent the output voltage and current variation with the change in the nMOS and pMOS channel length respectively. It is observed that output voltage increases with the increase in both the channel lengths, whereas the output current increases with the increase in Ln and falls with the increase in Lp.

The dependence of output voltage and current with channel width if both nMOS and pMOS is

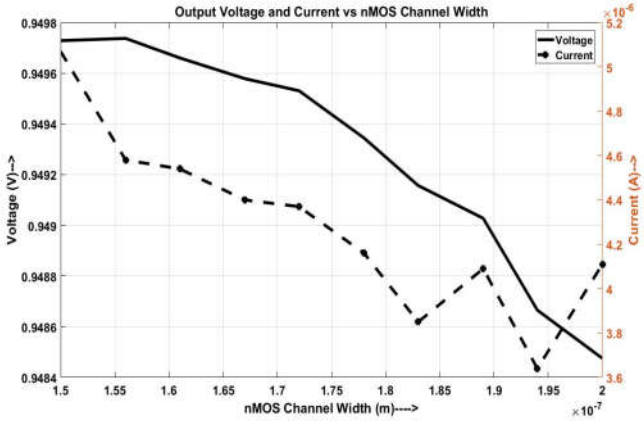

Figure 9: Output voltage and current vs nMOS channel width (W_n)

shown in the Figs.9 and Fig.10. Both the current and the voltages are seen to have a decline with the increase in W_n, whereas both the current and the voltage increases with the increase in W_p.

The frequency response of the circuit is evaluated. It is observed that the circuit can be operated in the complete RF band upto GHz mark. It can facilitate almost all types of RF transmission with high PCE and smoothly ensure energy harvesting in several known 3G/4G spectrum slots. This is shown in Fig.11.

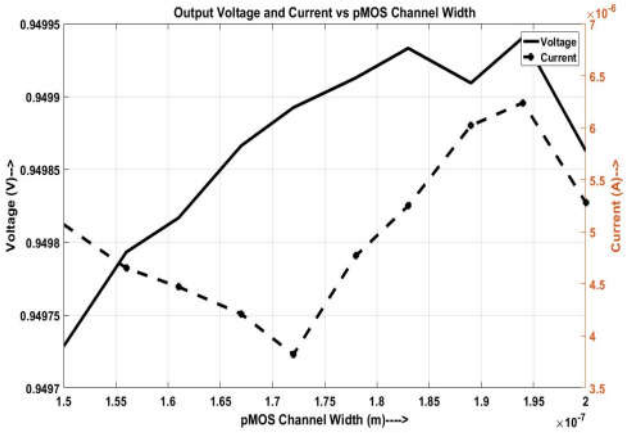

Figure 10: Output voltage and current vs pMOS channel width (W_p)

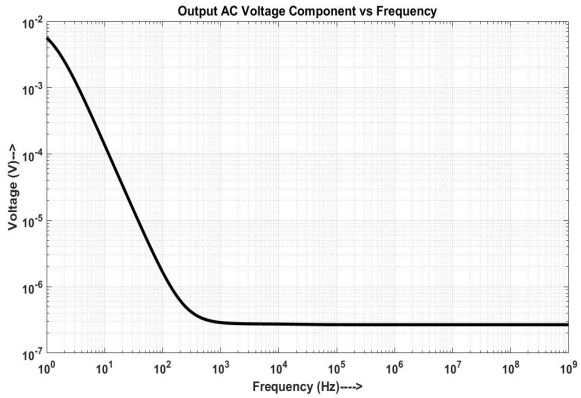

Figure 11: Output AC voltage component with frequency

The temperature stability of the circuit is another important aspect which needs to be investigated. The output AC component of the voltage is plotted against the temperature and it depicts that the AC component changes negligibly upto around 100^0 C and increases marginally beyond that temperature which is expected due to the rise in the leakage current. This is shown in Fig 12.

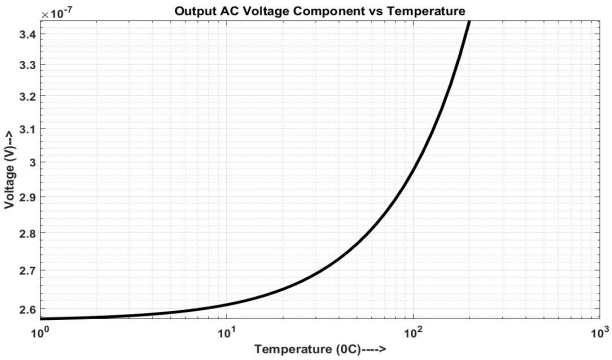

Figure 12: Output AC voltage component vs temperature

The output voltage and the current is plotted against the input power as shown in Fig. 13. Both the voltage and the current shows an increase with the input power.

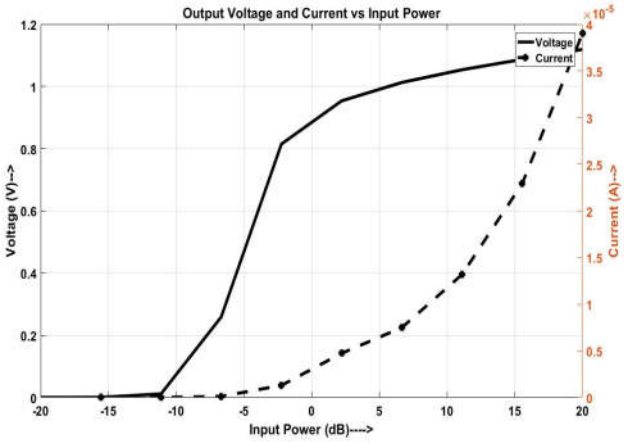

Figure 13: Output DC voltage and current vs P_{in}

Finally the PCE is calculated and plotted against a range of input power from -20dB to +20dB. The output DC voltage increases with input power. The maximum PCE is achieved to be 90% at -2dbm and 65% at -6dbm while the PCE is 60% at -8dbm. This is shown in Fig. 14.

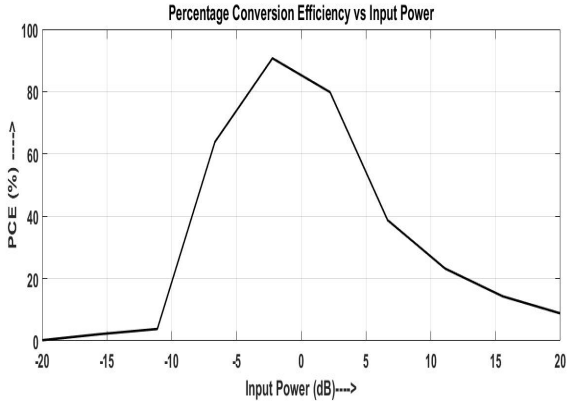

Figure 14: PCE vs P_{in}

The results obtained are compared with recently reported works by considering different parameters. This is presented in Table 2. The effectiveness of the proposed system is clearly evident.

Work	Comparison with the reported works					
	Technology	*Stage*	*Frequency (MHz)*	*Input Power (dbm)*	*Output Voltage (V)*	*Max PCE (%)*
[9]	Schottky Diode	1	868	10	-	48
[10]	Schottky Diode	1	900	-10	0.66	40
[11]	Schottky Diode	2	868	-10	0.649	44
[12]	Schottky Diode in 0.35 µm CMOS	5	900	-14.8	1.5	36
[13]	TSMC 0.18 µm	8	925	-21.2	0.78	43
[4]	0.18 µm CMOS	1, Diff	953	-12.5	0.62	67
[14]	TSMC 90 nm CMOS	5, Diff	868	-17	1.62	40
[15]	65 nm CMOS	5	900	18	6	31
[7]	65 nm CMOS	2	953	-15	0.402	56
[16]	45 nm CMOS	1	953	-2	0.485	80
This work	45 nm CMOS	2	953	-2	1.105	90

Table 2: Comparative Analysis

4 Conclusion

The 2-stage TG based rectifier with current boosting mechanism is presented in this paper. The design is evaluated for a wide range of frequencies upto GHz mark and is clearly found to be effective at almost all known commercially available 3G/4G bands for wireless networking. The maximum power conversion efficiency is achieved is 90% at -2db which is best in-class value as compared to the recently reported literatures. Hence the system can be suitably and effectively used as a core part of an energy harvesting system in a green communication set-up which will harvest the RF signal energy to an equivalent DC energy. The converted energy may be stored and even distributed to nearby nodes thereby making the nodes self-sufficient in terms of power. Optimal number of transistors are used in the design which makes the low area implementation possible. Thus the design can be said to be cost effective one as silicon is termed as the costliest real estate. The total dynamic power dissipation is 4.6µW. As power hungry designs are not suitable for this kind of applications, hence this parameter is very crucial. Finally it can be stated that the presented design achieves a significantly high PCE in almost all commercially available wireless bands with low power dissipation and comparatively lower silicon area. The challenge lies in the fact of achieving higher PCE at even lower input signal power which will make the design more versatile for real time applications. Also embedding the capability of multi-band harvesting is another milestone to be sought for.

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