Comparison of D flip-flops using Variability and Delay Analysis for Sigma Delta ADC

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Abstract: -Circuit with better robustness and minimum transistors is always preferred in a market to design a smart chip. Speed and variability of D flip-flop are required in sigma delta ADC to count the number of pulses after comparator. The paper aims to design single phase clocked feedback D flip-flop to achieve variability and delay by using minimum transistors. Instead of pass gate, the proposed circuit consists of feedback path isolation with inversion to lessen a number of transistors. It is compared with different kinds of D flip-flops that are used in sequential circuits. In this work, it is found that speed is better than Push pull isolation D flip-flop and robustness is quite good by minimum transistor. Circuit layout is built in Electric VLSI Cad Tool. Supply voltage of 0.9 V and 180nm technology is used.
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Key-Words: - D Flip-Flop, Delay, Variability, Speed, Robustness, Transistor

1 Introduction

Low power circuit design is an essential part of digital system. Sigma Delta ADC includes Integrator, comparator and DAC. In sigma delta ADC, after comparator D flip-flop is used to count the number of pulses [4] .Circuit with minimum transistor is required to accomplish this demand. So, various types of flip-flops are to be considered like TG based D flip- flop, TSPSC based D flip- flop, Low power D flip- flop, Push pull D flip- flop, Clocked D flip- flop and 10-T based D flip-flop etc.

D flip-flop is used in many VLSI circuits for clocking, microprocessors and converters etc. This flip-flop is a one bit memory cell and it is major part of sequential circuit for precisely performing on and off of signal. As per the truth table it produces output signal only on activation of clock signal and input signal. If clock is disabled, it returns the previous clock cycle output. Along with delay, other factor needs to be considered. This factor is variability. Variability is nothing but the ratio of standard deviation to mean of circuit delays. This factor makes transistor sensitive to PVT (process, voltage and temperature) changes [2]. Consequently, in order to satisfy above parameters requirement, simple circuit with single phase clocked feedback isolation D flip-flop is investigated in this paper. Results are compared with other types of D flip-flops [1].

2 Types of D flip-flop [3, 5]

In CMOS circuit, device parasitic decides the propagation delay [5]. It is nothing but the time required for the circuit to produce an output signal by the application of input. Propagation delay is measured of every flip-flop. From this Mean is calculated as

$$Mean = \frac{tplh + tphl}{2}$$

Further from Mean, standard deviation and variability are analyzed. Robustness of each circuit is observed.

2.1 TG (transmission Gate Flip-flop)

It is widely used type of flip-flop in many applications like sigma delta ADC, microprocessor etc. Fig.1.Shows circuit of TG flip-flop. It is built in a master –slave configuration. Master stage operates

on positive clock signal and slave operates on negative clock signal. On activation of positive clock signal D is passed to Q'. Similarly on activation of negative clock signal Q' is passed to Q. Further, based on deactivation of clock signal previous output is returned back at input of master and slave via TG switch to hold the same output signal. Rail to rail swing is good but it increase layout area.

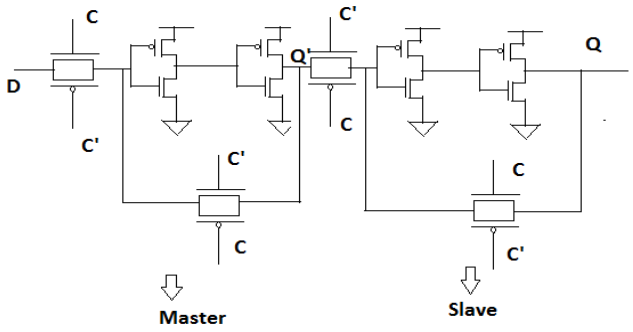

Fig.1 Transmission Gate Flip-flop [1]

2.2 TSPC (true single phase clock) D flip-flop

As depicted in Fig.2, it works on the clock signal equal to zero. It applies at C then based on value of D, it gives value of H low or high .It is the inverted signal of D input. Next X is inversion of H on activation of clock is equal to zero. Finally output is again inversion of X that is carried out from D to Q. During this M3 is off. During clock signal of '1', M3 will be on to pass the previous clock value of H to X as H holds previous value. Accordingly it holds again the previous output value at Q. Single phase logic is used in forward path which may create swing problem. Circuit is not robust well.

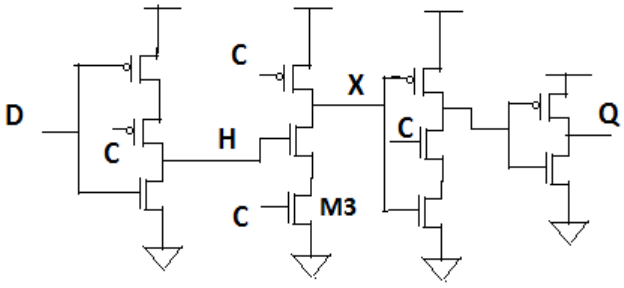

Fig.2 True Single Phase Clock D Flip-Flop [1]

2.3 Clocked CMOS D flip-flop

Now this circuit is working with C='1' as shown in Fig.3. If c is one the master carries input D and slave returns previous output to its input to hold constant output. Similarly if clock is zero, master returns previous output at Q to pass it to slave. So the output of slave is now stable till next condition. There is a swing problem by switching of one transistor at a time in forward path. So the circuit is not robust well again.

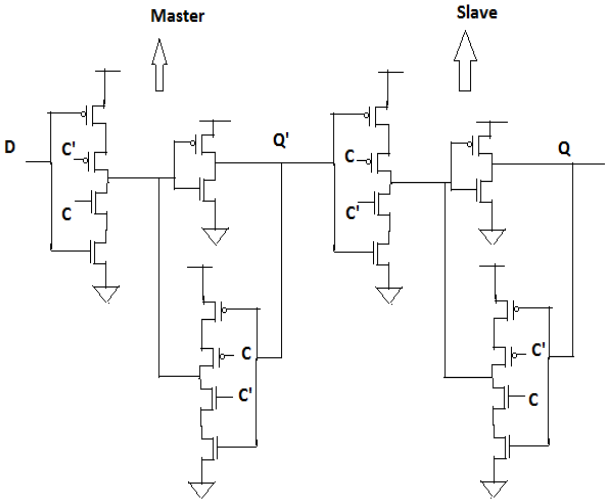

Fig.3 Clocked CMOS D flip-flop [1]

2.4 Ten transistor SET D flip-flop

As shown in Fig.4, if C is '1' then D value is passed to inverter hence X= D now. After disabling clock signal X is passed to Q via inverter and at the same time Q' is returned back to input inverter to properly maintain the stable value of Q until clock is equal to 1. Here is the great problem of swing as NMOSFET is used only for switching.

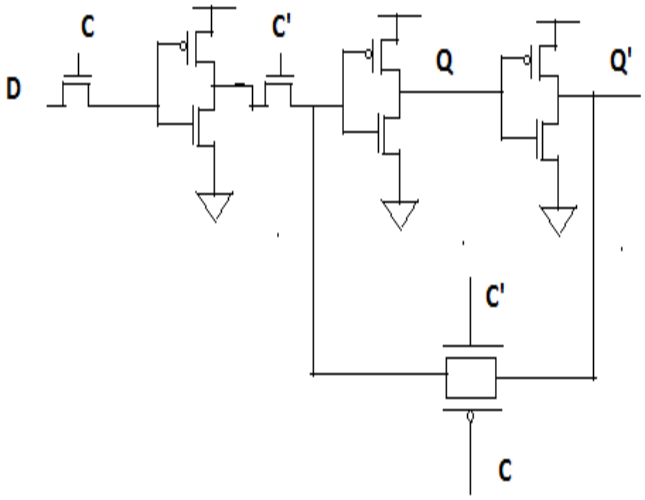

Fig. 4 Ten transistor SET D flip-flop [1]

2.5 Low power D flip-flop

Slight modification is done in Fig.1 to form a low power D flip-flop as shown in Fig.5. If clock is enable, D goes to input of inverter and on disabling on clock signal Q' is returned back to input of inverter. At same time Q' is passed to the slave input to produce output Q. Further, if clock goes to low level, output of slave Q is returned back at the input of slave. During this D again will go to the input of inverter to produce Q'. Simultaneously switching of two transistors will affect a robustness little bit. But circuit increases layout area.

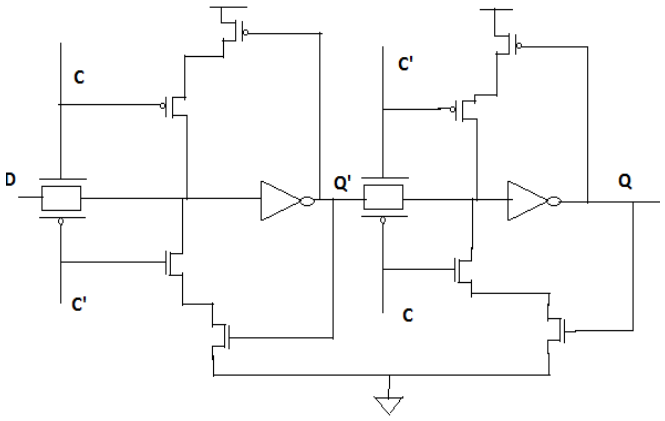

Fig. 5 Low power D flip-flop [1]

2.6 Push pull D flip-flop

Push pull D flip-flop is depicted in Fig.6.It shows push pull effect at slave. Once the clock is activated Q' takes the inversion of D and also return back this value at input of inverter. On disabling clock signal Q' is inverted to produce Q along with one additional path. This additional path creates stable value of Q and maintains it properly as it avoids clock to output delay. It increases layout area.

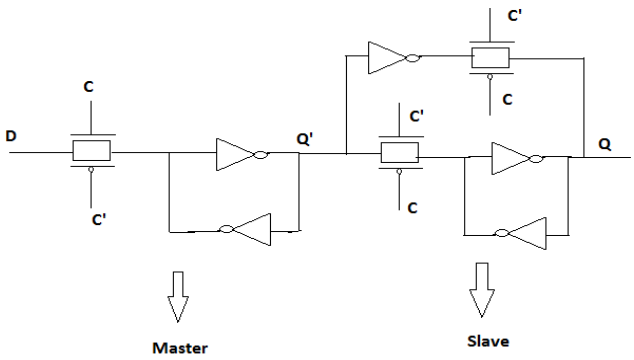

Fig.6 Push pull D flip-flop [1]

2.7 Push pull isolation D flip-flop

Modified structure of push pull is nothing but the push pull isolation D flip-flop as shown in Fig. 7.only one difference is noted in the feedback path. If clock is zero master output is stable and if clock is one slave output is stable by respective feedback path. This is more robust but it increases delay and area.

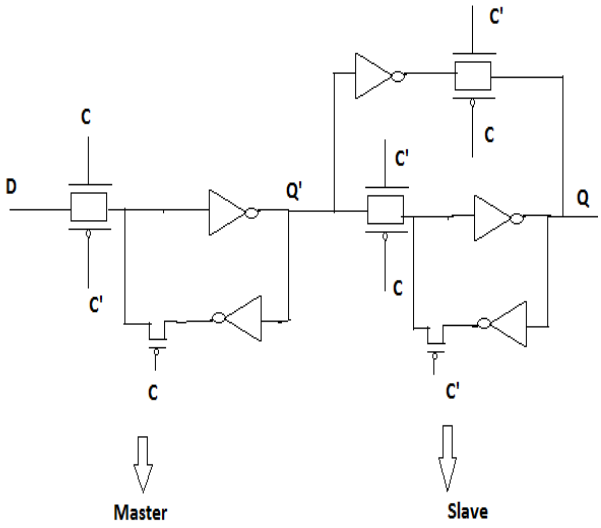

Fig. 7 Push pull isolation D flip-flop [1]

3 Proposed Single phase clocked feedback isolation type D flip-flop

Logic of D flip-flop with minimum transistor is designed to follow the truth table properly as shown in Fig.8. It creates the optimum delay and minimum variability. It consists of a single clocked feedback path with inverter and two transmission gates as a switch. To an N/P MOSFET as a switch, following equations of Ron and R are considered [1, 5].

$$Ron = \frac{1}{k\left(\frac{w}{l}\right)(Vgs - Vth)}$$

$$R = Rn\ II\ Rp$$

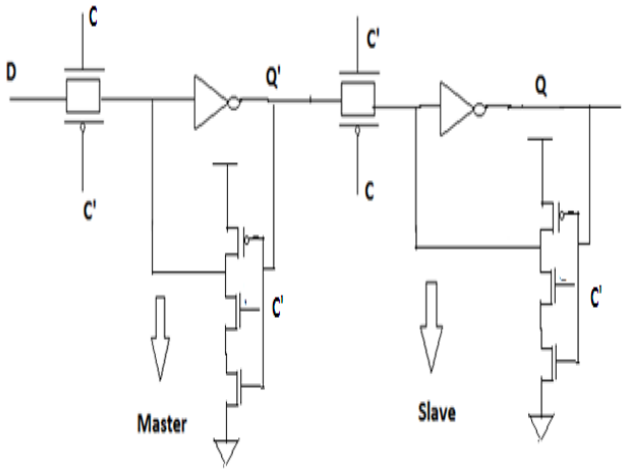

Fig. 8 Proposed D flip-flop

The aspect ratio is calculated by properly choosing the value of Ron. Proposed circuit is modified from push pull isolation D flip-flop. In this type feedback isolation is done using single MOSFET. This single transistor is not perfect switching to pass '0' and '1'. This imperfection is removed using a single clocked feedback path with inverter. In this type middle transistor is closed by single clock then either P or N transistor is closed based on input value. There is perfect '1' or '0' value passing from output to the input. Layout is drawn in Electric VLSI CAD Tool as shown in Fig. 9. Proposed circuit is verified for logic of D flip-flop. With condition of clock signal D is passed at input of transmission gate. Based on value of D output will be generated. On disabling of clock signal previous value of output is returned back at the input via switch to maintain stable output signal.

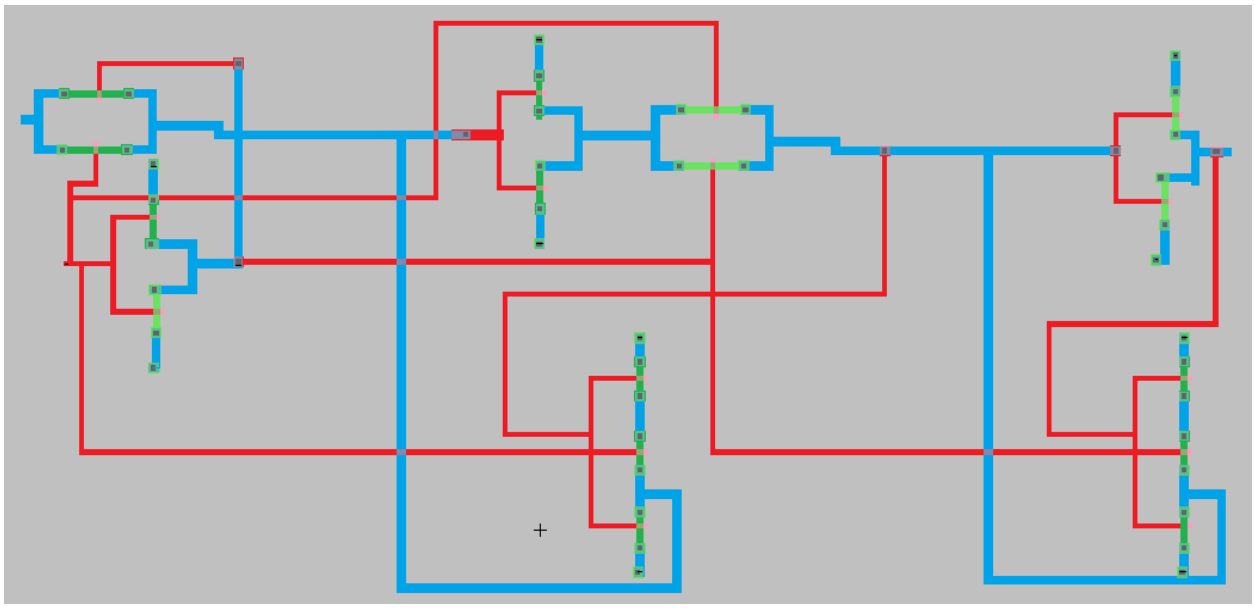

Fig. 9 Proposed D flip-flop Layout

4 Simulation Results and Discussion

Various D flip-flops are simulated by using 180nm technology. A spice net list is generated to check robustness. For maximum accuracy of the result Monte Carlo analysis is performed in 10% Gaussian variation. PVT (Process voltage Temperature) effect is prominently on the width(w),length(L), power supply (VDD), oxide thickness(*tox*) , channel doping concentration*(NDEP)*, and threshold voltage(*Vt*) parameters[3]. This effect is observed in the analysis for every circuit by using 3000 samples. In this paper, oxide thickness (*tox*), channel doping concentration *(NDEP)*, and threshold voltage (*Vt*) parameters are considered [1]. Speed of Clocked D flip-flop is good as mean value is 0.322ms but Robustness of Push pull isolation D flip-flop is good as variability is 2.788e-4. Mean delay of proposed type is 0.4296ms as summarized in the table 1, variability is 2.841e-4.Number of transistors required to design this logic are 14.Corresponding layout waveform is as shown in Fig. 10.

Table 1- Comparison of various types of D flip-flops

D flip- flop	Mean Delay(ms)	Std. Dev. of Delay(us)	Variability (Std. Dev./Mean)	No. of transistor
Single phase feedback Isolation D flip- flop	**0.4296**	**122**	**2.841e-4**	**14**
TG based D flip- flop	0.3712	232	6.238e-4	16
TSPSC based D flip-flop	0.3572	0.441	0.1247	11
Low power D flip- flop	0.4497	184	4.1e-4	16
Push pull D flip- flop	0.4441	225	5.05e-4	16
Push pull isolation D flip- flop	0.4996	139	2.788e-4	18
Clocked D flip- flop	0.3220	0.043202	0.1342	20
10-T based D flip-flop	0.3809	0.0191	0.05	10

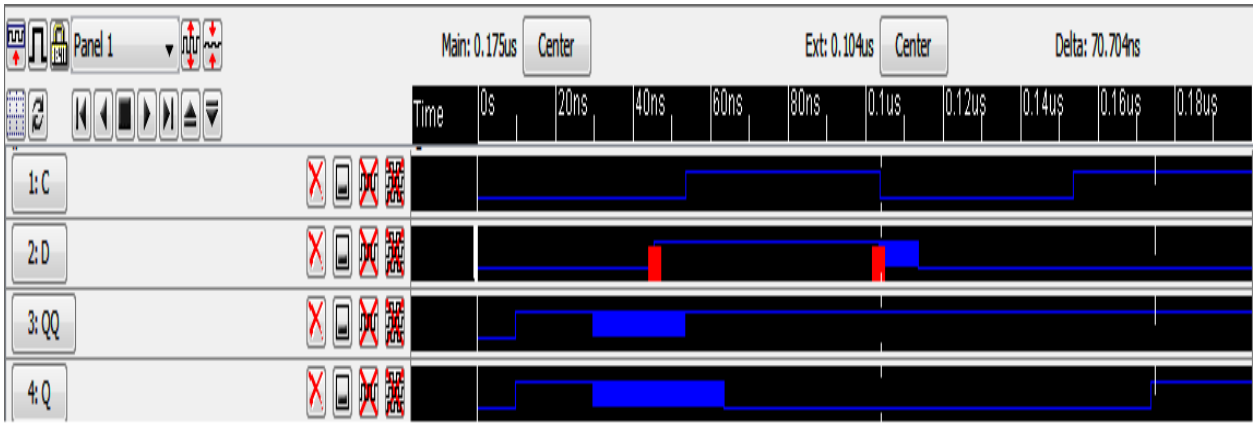

Fig.10 Waveform of proposed D flip-flop

5 Conclusion

The basic need of D flip-flop is studied for sigma delta ADC. All flip-flops are analyzed not only for the delay and robustness, but also for the number of transistors used. In conclusion, speed of single phase clocked feedback isolation is better than push pull isolation type by 14% because of low parasitic. Proposed type is approximately as good as push pull isolation type in robustness. Speed is good in clocked D flip-flop, but proposed circuit is much better in robustness by 99%. The circuit is simple to design with 14 transistors only as compared to all except 10T based D flip-flop and TSPSC based D flip- flop. This is one of the choices for designer based on the requirements of optimum delay, minimum variability and less area.

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