CMOS Customization of Comparator

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***Abstract*— In this paper, we present the customization methodology of high speed Flash ADC by optimizing its various components through CMOS channel length i.e comparator, so that the overall performance of the resulting Flash ADC or CMOS made device(s) is improved over traditional Flash ADC's. Together with high speed as a parameter, components are designed so that they operate with sampling frequency as high as 70-75 MHz with lowest power consumption and operate on power supply voltage down to 2V for compatible with low power digital portion of the design as well as occupy less chip area. All the components are designed using the 90 nm CMOS technology.**

Index Terms:Comparetor,Residue Amplifier,DAC

I.INTRODUCTION

In this paper, Flash analog to digital converters, also known as parallel ADC'S are used because they are the fastest way to convert an analog signal to digital signal. They are suitable for systems requiring very large bandwidths. However flash converters consume a lot of power, have relatively low resolution, and can be quite expensive .This limit them to high frequency applications that cannot be addressed in any other way. Examples include Data Acquisition, satellite communications, radar processing, sampling oscilloscope and high density disk drives. Two Step approach is the preferred design as it reduces area as well as power .High resolution with low area is achievable however at the expense of speed. The speed of the A/D and D/A interfaces must scale with the speed of the digital circuits in order to fully utilize the advantages of the advanced technologies. Recently low power ,compact size and high resolution analog –to – digital interface circuits have been in great demand for portable system such as camcorders ,cellular phones and personal digital assistance etc.High integration analog to digital interfaces for portable battery powered system require A/D converters and other interface elements that dissipate the lowest possible power and operate on supply voltages compatible with the digital parts of the system .Also the cost and performance makes it desirable to achieve high levels of integration on a single chip for mixed signal processing systems. In the previous years some of the high speed ADC 's have been designed using bipolar technology ,but the fabrication of these devices become very complex and large chip area and power .The motivation for CMOS is that higher levels of integration and low power are possible then in the bipolar implementation

II. TWO- STEP APPROACH OF FLASH ADC ARCHITECTURE

However, we have various architectures of Flash ADC'S as stated in the literature, but to achieve our main goals that is high speed and low power.,Two-Step architecture is used .Firstly, this architecture proves the speed of our ADC, may be a little bit , but the optimized components enhance the speed to a significant level..

In many applications it is necessary to have a smaller conversion time.ADC..ADC's designed for such applications are the high speed ADC's that use the parallel techniques to achieve the shorter conversion times. One way of achieving this is to increase the speed of the individual components, which will increase the speed of the complete system. Sample time due to the sample and hold circuit may be a limiting factor for the speed. We proceed to design a system without sample and hold circuit.

The potential of two-step flash architectures for realizing fast, high resolution analog to digital converters are demonstrated in a number of designs [4] [6] [7]. With the conversion rates approaching half those of fully parallel (flash ADC) these architectures provide relatively small input capacitances together with the low power dissipation and can be used to achieve resolutions in the range of 10 to 14b which is well above that obtained in the single stage flash designs. The basic structure of the two-step converter is shown in Fig. 1.The first converter generates a rough estimate of the value of the input, and the second converter performs a fine conversion. The advantage of this architecture is that the number of comparators is greatly reduced from that of the flash converter from 2^N-1 comparators to $2(2^N-1)$ comparators. For example, an 8 bit flash converter requires 255 comparators, while the step requires only 30.The tradeoff is that the conversion process takes two step instead of one, with the speed limited by bandwidth and settling time required by the residue amplifier and the summer

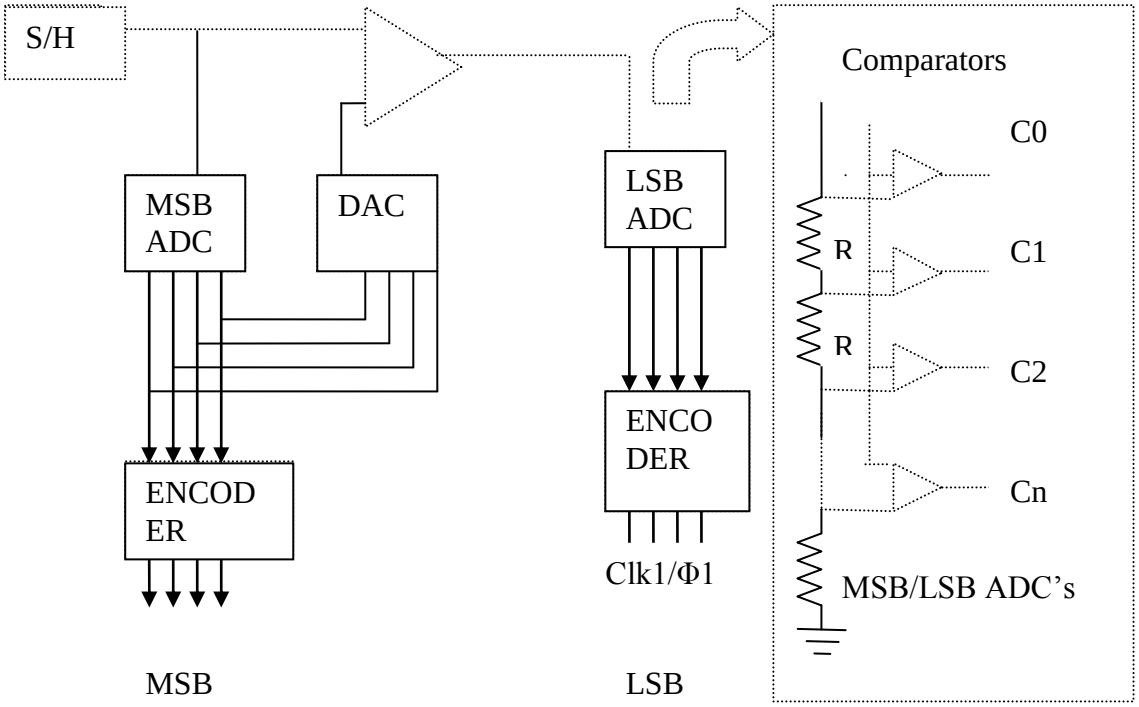
III. ADC COMPONENTS OPTIMIZATION

To improve the speed we optimize the different components of the ADC individually and independently.
The architecture of the different components of ADC are chosen so that when they are cascaded together they enhance the speed significantly.

Comparator Design: In high speed analog to digital converters, comparator design has a crucial influence on the overall performance that can be achieved.Conveter architecture that incorporate a large number of comparators in parallel to obtain a high throughput rate impose stringent constraint on delay, resolution, power dissipation, input voltage range that accompany the integration of comparator circuits in low-voltage scaled VLSI technologies,severly compromise the precision that can be obtained.

A high performance comparators need to amplify a small input voltage (the difference between the input voltage and the reference voltage) to a level large enough to be detected by the digital logic circuits within a very short time. In its simplest form, the comparator can be considered as a 1 bit analog to digital converter. Comparators can be divided into

open loop and regenerative comparators The open loop comparators are operational amplifiers with out compensation.Regenrative comparators use positive feedback, to accomplish the comparison of the magnitude between two signals



Residue Amplifier

Fig. 1.Two-Step Flash ADC Architecture

The comparator design used for the A/D application is based on [2][5][6] .This is shown in Fig. 2.Operating analysis of the comparator is as given by [5][2].Finally, by further reducing and solving the inequalities we obtain the relation $W_{12}>1/3W_4$.Similarly other relations are calculated at node c&d.

Single Cell DAC Circuit Design:
Digital to analog converter is the integral part of any ADC. There are a number of means of converting a digital signal into an analog signal representation. The approaches differ in speed chip area, power efficiency, and achievable accuracy etc.It is therefore necessary to understand which converter algorithms or architectures to choose for the specific application. For Working of the single current cell: Here the transistor MS1,MS2 and MS4 act as the switch, the control of which is governed by the output of the comparator. The transistor MD1 and MD2 are used for the fast charging and discharging of M2, M3,the transistor M1 is used as a constant current source, which is biased such that all the time it can handle the maximum current. When the comparator output comp is high and compb is low, switch made by the MS1 and MS2 is ON and hence M2 is ON and a some current would flow through Rout and the corresponding value of the output voltage will be generated. The same operation is true for M3,when the comp is low and compb is high. Current supplied by all the cells are of the equal magnitude

Differential Amplifier/Residue Amplifier Design:
The last circuit of our ADC is Differential amplifier .It is used as a subtracter amplifier. Simple circuit of differential amplifier is used as shown in Fig. 4.. example when the conversion bandwidth is relatively small, it could be advantageous to use a high sampling ratio and some overlapping technique to reduce the noise energy within the signal band. However the trade off in the converter design is normally between resolution and bandwidth. The higher the bandwidth the lower the resolution and so on. One of the most suitable candidate for high speed and high resolution is the current steering DAC.The Single Cell of our DAC has the structure as given in Fig.3.Single cell of the DAC corresponds to 1-bit DAC.To design a full functional DAC we have to combine these cells together with the regulator circuitry.

IV.RESULT AND DISSCUSSION

The main purpose of our design is to achieve high speed with low power. . To achieve this .T-Spice code of the individual components has been made using Tanner tools .The W/L ratios of all the transistors of the components design are calculated using the design relations developed as mentioned and using the model parameters of 90 nm technology of Tanner Tool. The output waveforms obtained of different components are shown in Fig.5, Fig.6, Fig.7.Referencevoltage is taken constant. Parameters specification obtained are shown in Table 1.1.

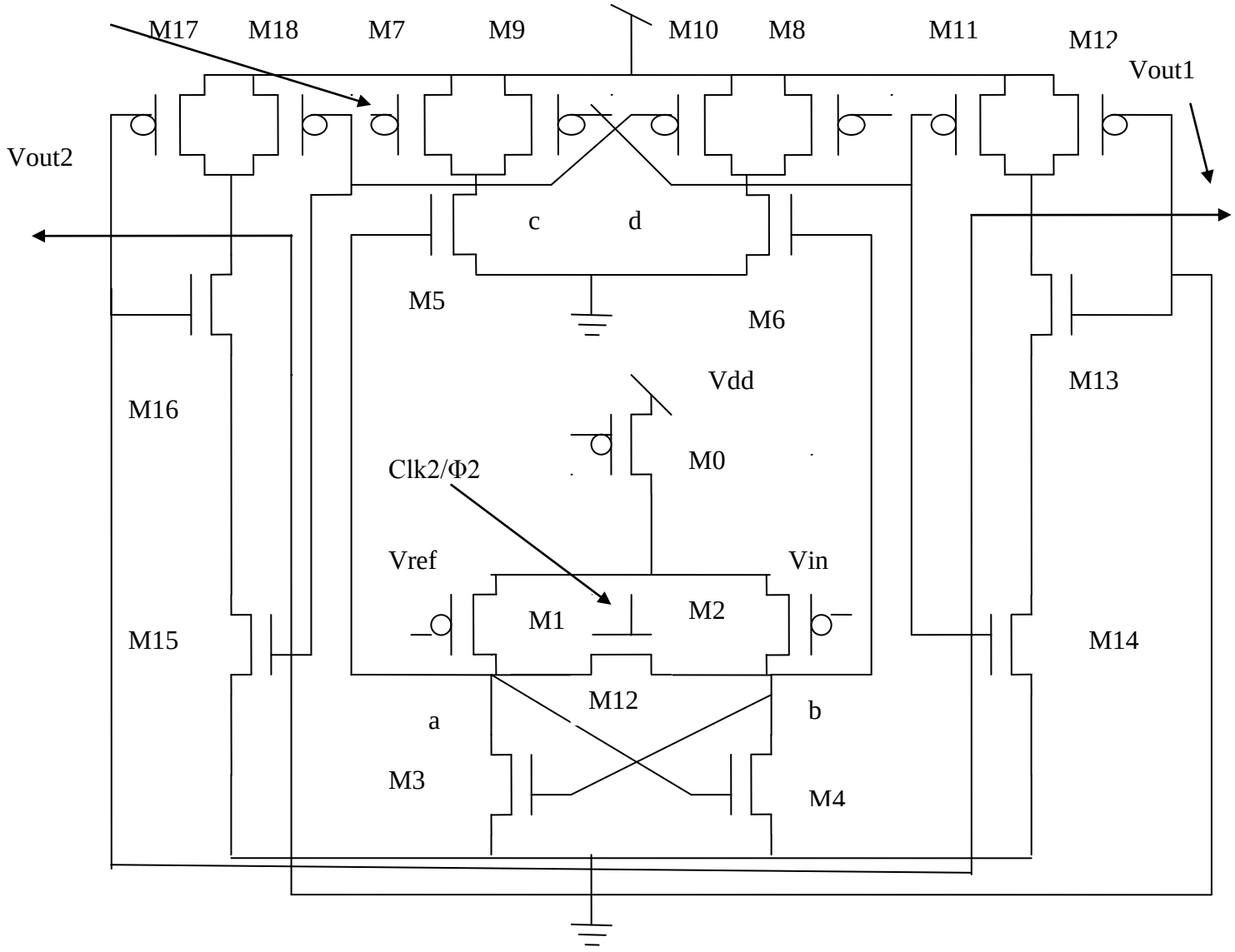


Fig 2 Comparator Circuit

Table 1.1 Parameter Specification for complete ADC

Resolution	8-bits
Input Signal Frequency	2MHz
Sampling Frequency	70-75MHz
Technology Used	90 nm
Analog input (Ref. Volt.)	0-1V(P-P) (0.8-1.6V)
Power Supply	2V

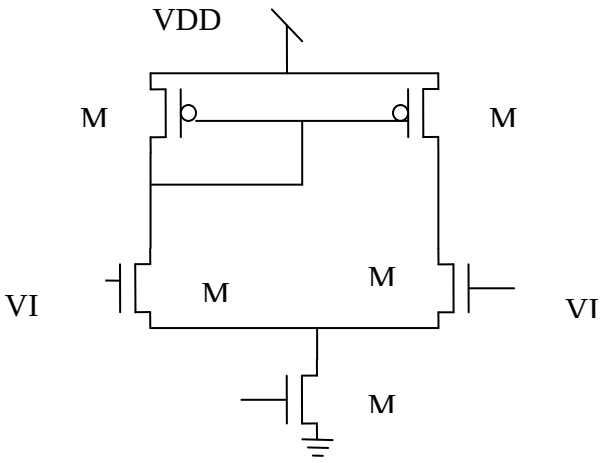


Fig.4.Differential Amplifier/Residue Amplifier

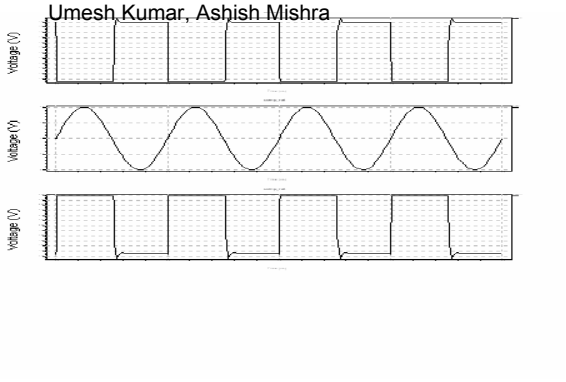


Fig.5 Comparator output for Vref=0.125V

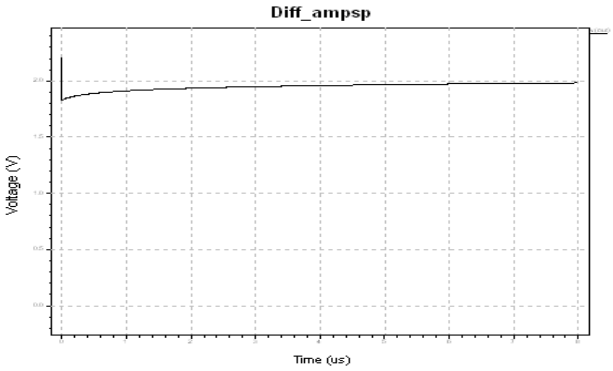


Fig.6 Output of Residue Amplifier

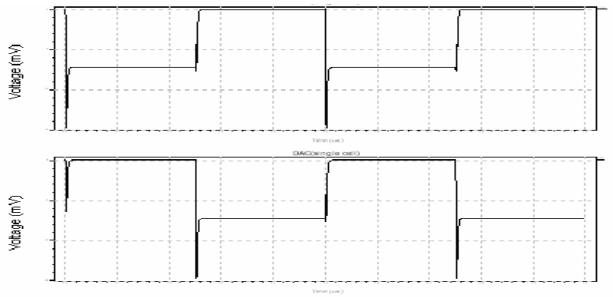


Fig. 7 Output of Single Cell DAC(1-bit)

V. CONCLUSION

The work presented in this paper is to design and analyze the performance characteristics of the two-step flash ADC components. For this design technique are developed for individual components of the ADC.Based on the scheme developed W/L ratios for all the transistors are calculated using the model parameters of the 90 nm CMOS technology. Individual components are implemented independently. The preferred technology as with the scaling of operating voltages to low values down to 2V, it ensures a high performance circuit. The designed components are best suited for a complete flash ADC

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