A High Performance D-Flip Flop Design with Low Power Clocking System using MTCMOS Technique

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Abstract—**Power consumption plays an important role in any integrated circuit and is listed as one of the top three challenges in International technology roadmap for semiconductors. In any integrated circuit, clock distribution network and flip -flop consumes large amount of power as they make maximum number of internal transitions. In this paper, various techniques for implementing flip–flops with low power clocking system are analyzed. Among those techniques clocked pair shared flip-flop (CPSFF) consume least power than conditional data mapping flip flop (CDMFF), conditional discharge flip flop (CDFF) and conventional double edge triggered flip-flop(DEFF). We propose a novel CPSFF using Multi-Threshold voltage CMOS (MTCMOS) technique which reduces the power consumption by approximately 20% to 70% than the original CPSFF. In addition, to build a clocking system, double edge triggering and low swing clocking can be easily incorporated into the new flip-flop.**

Keywords- flip-flop; low power integrated circuit; power delay product; MTCMOS.

I. INTRODUCTION

In the past area, performance, cost and reliability were the main concerns for VLSI designer and power consumption was secondary consideration. In recent years, however, this has begun to change rapidly and power is being given equal importance in comparison to area and speed [1].Ever increasing demand for mobile electronic devices and remarkable success and growth of the class of wireless communications systems as personal digital assistants and personal communicators which demand complex functionality and high speed has increased the requirement of the use of power efficient VLSI circuits.

There are three major sources of power dissipation in digital circuits which are summarized in the following equation [2]

$$P_{avg} = P_{switching} + P_{short\text{-}circuit} + P_{leakage} = \alpha C_L V_{dd}^2 f_{clk} + I_{sc} V_{dd} + I_{leakage} V_{dd} \quad (1)$$

The first term represents the switching component of power, where C_L is the load capacitance, f_{clk} is the clock frequency and α is the probability that a power consuming transition occurs (the activity factor).The second term is due to the direct-path short circuit current, I_{sc}, which arises when both the nMOS and pMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and sub-threshold effects, is primarily determined by fabrication technology considerations.

As technology scales down, the short circuit and leakage power becomes comparable to dynamic power dissipation [3][4].Consequently, the identification and modeling of different leakage and switching components is very important for the estimation and reduction of power consumption especially for high-speed and low-power applications. Multi-Threshold voltage based CMOS (MTCMOS) technique and voltage scaling are two of the low power techniques used to reduce power consumption.

Flip-Flop is an electronic circuit that is used to store a logical state of any data input signals with the response to a clock pulse. Flip-flops are widely used to receive and maintain data in selected sequences during reoccurring clock intervals for a limited time period sufficient for other circuits within a system. A huge portion of the on chip power is consumed by clock systems, which consists of timing elements such as flip-flops, latches and clock distribution network.These clock systems have redundant transition and the transition probability of the clock is 100% while an ordinary logic has one-third on average so clock systems are one of the most power consuming components in a VLSI system [1]–[5].These components consume 30% to 60% of the total power dissipation in a system [2].Consequently, reduction in the power consumed by flip-flops will show a deep impact on the total power consumed.

Several techniques as well as various flip-flops have been proposed recently to reduce redundancy in clock system. There are many flip-flops given in the literature [5]-[12]. Many digital and computational circuits selectively use master-slave and pulsed-triggered flip-flops [2]. There are two types of edge triggered flip-flops given in literature hard edge (transmission gated edge triggered flip-flops and sense amplifier-based flip-flops) and soft edge (pulse-triggered flip-flops).The hard edge triggered flip-flops consist of two stages,

one master and one slave which cause large D-to-Q delays and are characterized by a positive setup time. Alternatively, soft edge triggered flip-flops reduce the two stages into one stage. The classification of the pulse triggered flip-flops can be made in two ways, first being explicit-pulsed triggered and the other being implicit-pulsed triggered flip-flops.As the pulse generator in the case of explicit flip-flops is present externally thereby sharing of the pulse generator in this case becomes feasible than in the case of the implicit-flip flops where the pulse generator is internal to the circuit. The sharing in the case of explicit-pulse triggered flip-flops can help in distributing the power overhead of the pulse generator across many flip-flops so to have the advantage of better performance since the height of the nMOS stack in this case is less than that in the implicit flip-flops [3].

This paper is organized as follows. Section II surveys various flip-flops for low power design. Section III describes MTCMOS technique for the abatement of standby leakage power consumption. Section IV presents the proposed Multi-Threshold CPSFF (MT-CPSFF) for low power and better performance. Section V presents simulation results. Section VI concludes this paper.

II. Techniques for Reducing Clock Activity

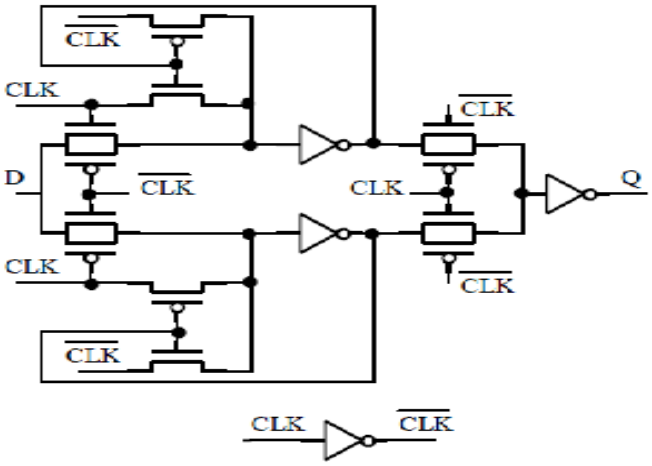
We survey various D flip-flops and categorize them into four different groups as shown in the Fig. 1: conventional double edge triggered flip-flop (DEFF), conditional discharge flip-flop (CDFF), conditional data mapping flip-flop (CDMFF) and clocked pair shared flip-flop (CPSFF).

Fig. 1(a) [6] shows that DEFF samples the data both at the rising and the falling edge of the clock signals. It has the same number of transistors as that of the conventional single edge triggered flip-flop (SEFF) [6]. Reduction of the frequency to half in case of DEFF results in abatement of the power dissipation to approximately half of the value of SEFF.

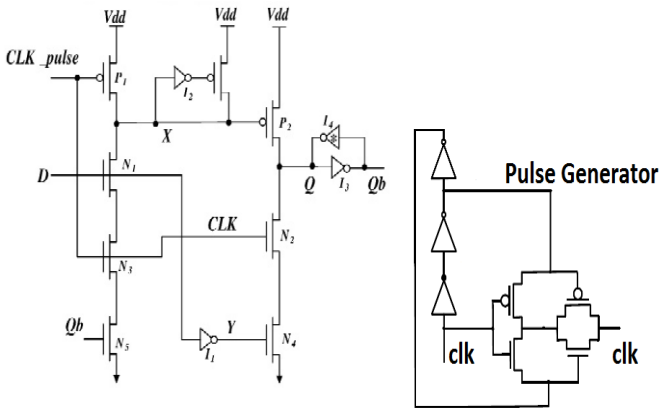
CDFF is suitable for both implicit as well as explicit pulse triggered flip-flops. CDFF uses a pulse generator which eventually generates the pulses for implementing the circuit in double edge triggered technology. As shown in Fig. 1(b) [7] CDFF operates in two stages. The first stage is mainly for the LOW to HIGH transition, while the second stage being responsible for HIGH to LOW transition. Removal of extra switching activity takes place by controlling the discharge path when the input is at stable level '1'.Controlling of the discharge path results by adding nMOS which is controlled by Qb. The discharge path of the first stage helps in preventing evaluation in the coming clock cycles as long as input remains at stable level '1'[7].

CDMFF uses pulse–triggered structure for high performance in contrast to CDFF which uses double edge clocking. As shown in Fig. 1(c) [2] CDMFF uses only 7 clocked transistors in comparison with CDFF which uses 13 clocked transistors resulting in reduction of the power consumption. The conditional data mapping (CDM) methodology exploits the property of the flip-flop, by providing the flip-flop with a stage to map its inputs to (0, 0) if a redundant event is predicted, such that the outputs will be unchanged when clock signal is triggered .A conditional data mapper is deployed in the circuit to map the inputs by using outputs as control signals. CDMFF outperforms CDFF in terms of power consumption [9]-[11].

Although CDMFF reduces the power consumption but it is more susceptible to redundant clocking in addition to a floating node [9]. CPSFF overcomes the problem of floating node in CDMFF by reducing the number of clocked transistors as shown in Fig. 1(d) [12]. CPSFF uses 4 clocked transistors in comparison with CDMFF which uses 7 clocked transistors; thus reducing the clock load. In CPSFF the clocked pair is shared by the first and second stage. The always on pMOS in CPSFF allows the internal node to be always connected to V_{dd} thus prevents the floating problem. Thus in terms of power consumption of clock circuit CPSFF is more efficient than CDMFF.



(a)



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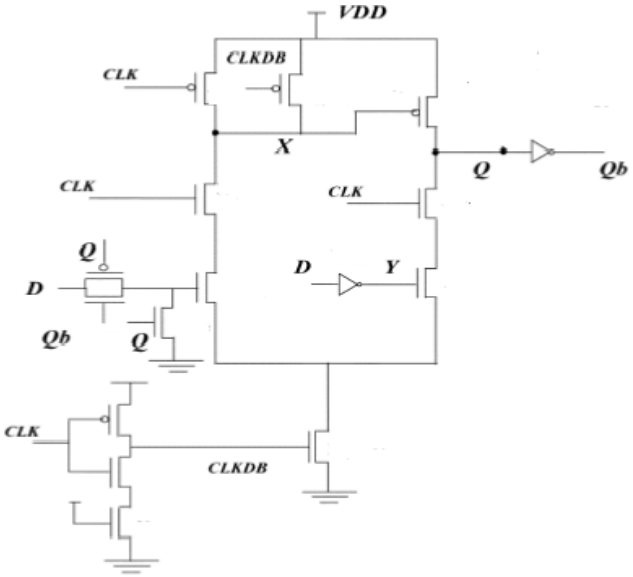

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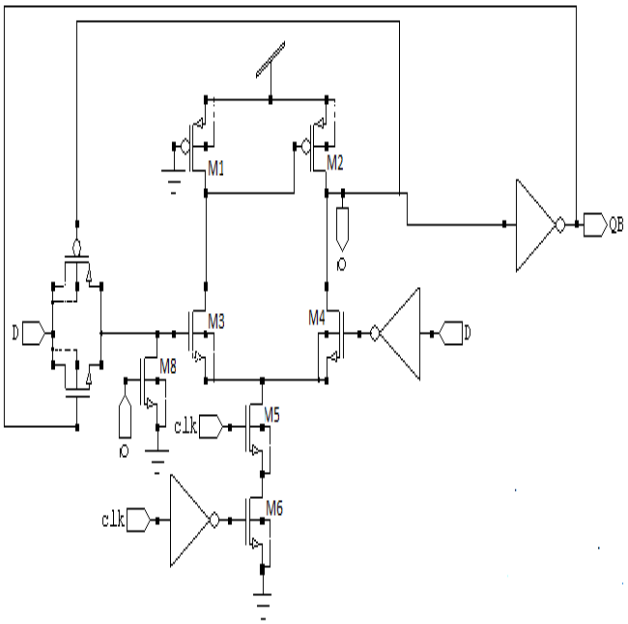

(d)

Figure 1. (a) DEFF. (b) CDFF. (c) CDMFF. (d) CPSFF.

III. MTCMOS TECHNIQUE

Supply and threshold voltages are reduced with the scaling of CMOS technologies. Lowering of threshold voltages leads to an exponential increase in the sub threshold leakage current. In modern high performance integrated circuits (ICs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. With more transistors integrated on-chip, leakage currents will soon dominate the total energy consumption of high performance ICs. Furthermore, leakage current is typically the only source of energy consumption in an idle circuit.

The battery-powered portable applications such as cell phones and laptop computers tend to have long standby modes. Reducing the leakage energy consumption of the portable devices during these long idle periods is highly desirable for a longer battery lifetime. A popular low leakage circuit technique is the Multi-Threshold Voltage CMOS (MTCMOS).

The MTCMOS technology has two main features. First, "active" and "sleep" operational modes are associated with MTCMOS technology, for efficient power management. Second, two different threshold voltages (V_t) are used for N channel and P channel MOSFET in a single chip [13]. This technique based on disconnecting the low threshold voltage (Low-V_t) logic gates from the power supply and the ground line via cut-off high threshold voltage (High-V_t) sleep transistors is also known as "power gating" and is an effective technology to achieve higher performance as well as smaller stand by leakage current. MTCMOS technology is based on using two different kinds of MOSFETs with two different threshold voltages (Low V_t and High V_t) respectively. The low V_t MOSFETs enhance the speed performance while the high V_t reduces the stand by leakage current [14], [15].

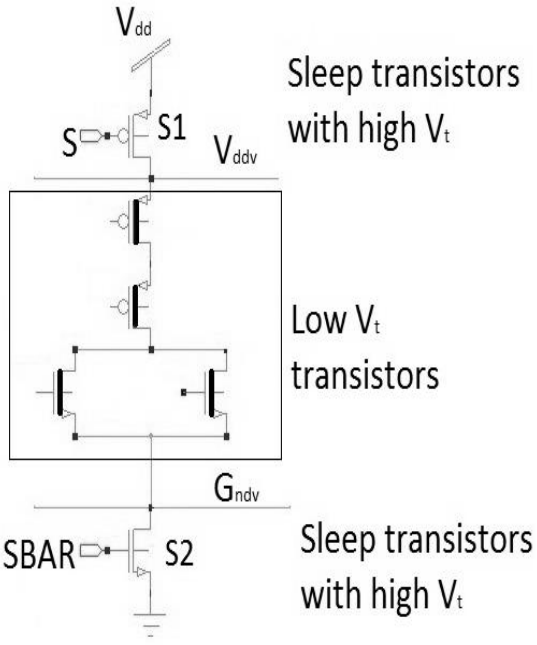

Figure 2. Power gating technique using MTCMOS.

The schematic of power gating technique using MTCMOS is shown in Fig. 2. This schematic consists of two sleep transistors S1 and S2 with higher V_t. The logic circuit between the S1 and S2 is not directly connected to real supply lines V_{dd}

And G_{nd} but in turn it is connected to virtual power supply lines V_{ddv} and G_{ndv} and has low V_t. Both the sleep transistors are given complementary inputs S and SBAR. The above circuit operates in two modes active mode and standby mode.

In active mode, S=0 and SBAR=1 such that S1 and S2 are ON and virtual supply lines V_{ddv} and G_{ndv} work as real supply lines therefore the logic circuit operates normally and at a higher speed. In sleep mode, S=1 and SBAR=0 such that S1 And S2 are OFF and this will cause virtual power supply lines to float and large leakage current present in circuit is suppressed by sleep transistors S1 and S2 resulting in lower leakage current and thus reducing power consumption.

IV. PROPOSE CLOCK PAIR SHAIRED FLIP FLOP USING MTCMOS

To reduce standby leakage power consumption and to ensure efficient implementation of sequential elements, we propose clocked pair shared flip-flop using MTCMOS technique. We are designing this circuit keeping the number of clocked transistors same as in the actual circuit. The schematic of MT-CPSFF is shown in Fig. 3.

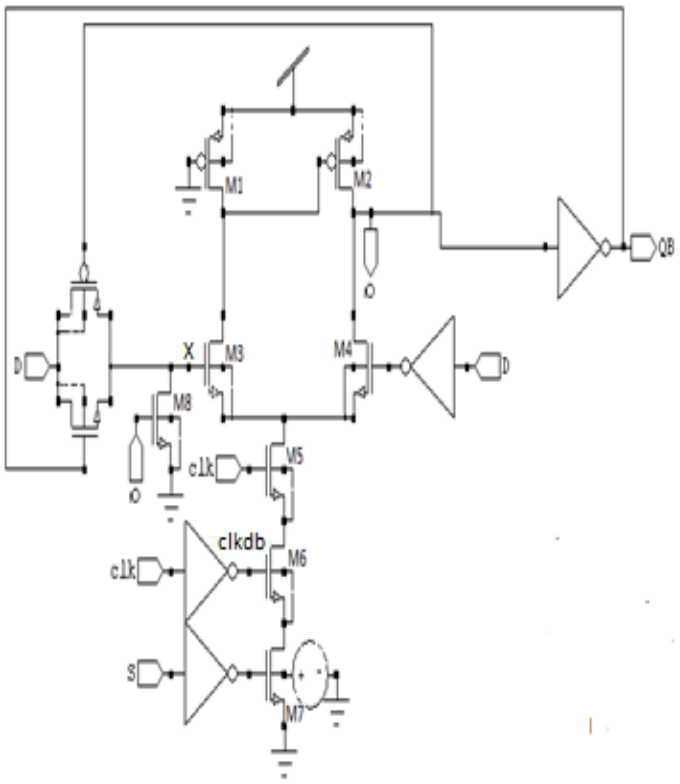

Figure 3. Schematic of Proposed CPSFF using MTCMOS.

In this proposed Clocked Pair Shared Flip Flop, a high threshold voltage nMOS transistor is provided with a sleep signal S,which is high in the active mode and low during the standby mode.

Here, the first and the second stage shares the same clocked pair(M5 and M6).Furthermore,the pMOS M1 is always turned on and is connected to the power supply V_{dd}, thus charging the internal node X all the time .This reduces the floating of node X and enhances the noise robustness.

The flip flop works, when both clk and clkdb are at logic '1'. Psuedo nMOS and conditional mapping technique both are combined using the above scheme. The nMOS M3 is controlled by a feedback signal. For input D=1and S=1,Q will be high, swtiching ON the transistor M8,and turning OFF M3 thus parrying redundant switching activity and flow of short circuit current at the node X. When D transits to 1 the output Q is pulled up by pMOS M2 whereas M4 is used to pull down Q when D=0 and Y=1 at the arrival of clock pulse.

When the input D transits from 0-1 the short circuit occurs for once even though M1 is always ON,thus disconnecting the discharge path and turning off M3 after two gates delay by feedback signal. There will be no short circuit even if the input D stays high as M3 disconnects the discharge path.The output of the flip flop depends upon the state previously acquired by Q and QB along with the clock and the data signal inputs provided[12].

V. SIMULATION RESULTS

The simulation results for all existing and proposed flip-flops were obtained in a 90nm CMOS technology at room temperature using Tanner EDA Tools 13.0 over various supply voltages and frequencies. Table I shows power comparison results for the DEFF, CDFF, CDMFF, CPSFF and the proposed MT-CPSFF for 1.5, 2.5 and 3.5 supply voltage(V_{dd}) over 750MHz and 500MHz clock frequencies. Table I shows that CDFF has 38% less power consumption than conventional DEFF at 750MHz clock frequency and $1.5V_{dd}$.Similarly at 500MHz and $3V_{dd}$ CDFF consumes 74% less power than conventional DEFF. Since the clocked transistors in CDFF is more as compared to 7 clocked transistors in CDMFF, the power consumed by the later at 750MHz and $1.5V_{dd}$ is 81% less as compared to the former. Albeit CDMFF reduces the power consumption to a considerable amount but it is susceptible to redundant clocking in addition to a floating node.

The CPSFF overcomes this drawback by reducing the number of clocking transistors. For 500 MHz and at $3V_{dd}$ CPSFF consumes 53.8% less power than CDMFF. Similarly at 750MHz and $1.5V_{dd}$ CPSFF consumes 9.74% less power as compared to CDMFF. The comparison shows that reducing the clocked transistors has a major effect on reducing the total power consumption of the design circuit.

The proposed MT-CPSFF which makes use of MTCMOS technique shows higher performance as well as smaller standby leakage current. The low V_t MOSFETs enhances the speed, while the higher V_t MOSFETs reduces the standby leakage current.

TABLE I POWER CONSUMPTION COMPARISON FOR VARIOUS FLIP-FLIPS

Design Name	Area (Number Of Transistors)	100% Switching Activity Transistor	Frequency					
			500MHz			*750MHz*		
			Powers Consumption(µW)			*Powers Consumption(µW)*		
			Supply Voltage (V_{dd})					
			1.5v	2.5v	3v	1.5v	2.5v	3v
Conventional DEFF	24	12	18.3	119	211	23.7	132	231
CDFF	26	13	9.74	36.4	54.8	14.6	53.9	82.0
CDMFF	20	7	1.98	19.4	49.6	2.77	22.1	53.7
CPSFF	17	4	1.39	15.0	22.9	2.50	22.1	32.8
MT-CPSFF	21	4	1.23	4.47	7.70	2.12	5.78	11.6

Table I shows that for MT-CPSFF at 500MHz and $3V_{dd}$, the proposed circuit consumes 66.3% less power as compared to conventional CPSFF. Similarly at 750MHz and $1.5V_{dd}$ MT-CPSFF consumes 15.2% less power than conventional CPSFF.

VI. CONCLUSION

In this paper, a new design for D flip-flop is introduced to reduce internal switching activity of nodes and stand by leakage power; along with this variety of design techniques for low power clocking system are reviewed. This proposed flip-flop reduces local clock transistor number and power consumption as well. The proposed MT-CPSFF outperforms previously existing DEFF, CDFF, CDMFF and CPSFF in terms of power and good output response by approximately 20% to 85%. Furthermore, several low power techniques, including low swing and double edge clocking, can be explored to incorporate into the new flip-flop to build system.

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