A Fully Optimized Ultra Wideband Mixer in 65nm CMOS Technology

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Abstract: - This paper presents the design and analysis of Ultra Wideband (UWB) mixer in 65nm CMOS technology. To achieve the optimized performance, a new mixer topology is suggested. The performance parameters of the mixer viz.: conversion gain, Noise Figure, linearity and power consumption are addressed in this paper. The simulation results of the new mixer topology suggested in this paper achieves the reasonably good conversion gain (CG) of 7.27 – 10.92dB, a third order intercept point (IIP3) of +2.01 to +6.7dBm and Noise Figure (NF) of 10.4 to 12.4dB between entire band of 3.1-10.6GHz while consuming only 3.6mW of power from 0.8V supply.

Key-Words: - Ultra Wideband, Noise Figure, IIP3, Gilbert Mixer, CCPDT, Conversion Gain, UMC

1 Introduction

The Federal Communication Commission (FCC) in 2002 allocated 7.5GHz of spectrum for unlicensed use of Ultra Wideband (UWB) technologies in the 3.1 to 10.6GHz frequency band [1]. UWB technology (IEEE 802.15.3a) is suitable for high rate data communication for short range. Its bandwidth of 7.5GHz is divided into 14 channels with a bandwidth of 528MHz. In addition, each band is composed of 128 sub-channels with a channel bandwidth of 4.125MHz. Fig. 1 shows the band structure of MB-OFDM UWB application. The first 12 bands are then grouped into four sub band groups, each consisting of three bands, and the last two bands are grouped into the fifth band group.

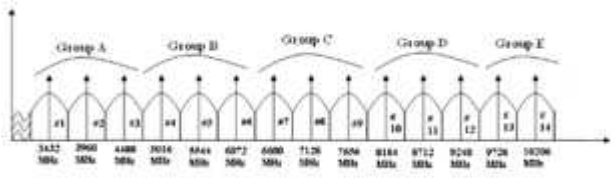

Fig.1: Frequency Plan of MB-OFDM UWB

Fig. 2 shows the block diagram of UWB direct conversion receiver (DCR). Mixer is an essential building block in receiver frontend used for frequency translation. The down conversion mixer in DCR system is critical block because it leads noise figure and linearity of system. Linearity of the whole receiver is dominated by mixer. Nonlinearity causes many problems like gain compression, distortion and desensitization. Differential architectures of mixer can easily filter out the even order nonlinearity but odd order nonlinearity is difficult to remove, especially the third order inter-modulation distortion. In addition to linearity, the

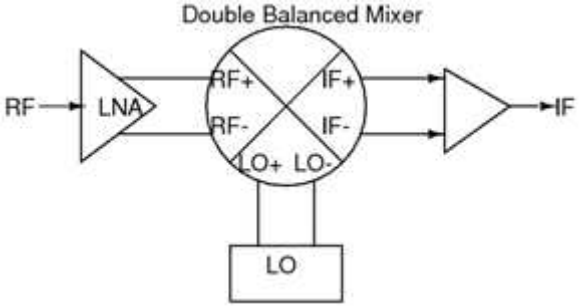

Fig. 2: Block diagram of Receiver Front end

Other performance parameters of the mixer like Conversion Gain (CG), Noise Figure (NF), port isolation and power dissipation are also very important at high frequency especially over the bandwidth (7.5GHz) of UWB systems.

This work reports a design of Gilbert cell mixer in standard UMC 65nm MSRF CMOS technology. The process is set for 1P8M1T0F with one poly layer for gate of MOS and eight metal layers for interconnections [2]. The metal option_26 is used which has high quality (Q) inductor and MIM capacitor. The voltage option is set to 2.5V. The mixer reported in this work is fully optimized to give high linearity and low noise figure while

consuming low power. This paper is organized as follows. Section 2 presents the analysis and discussion on conventional Gilbert mixer and Folded Gilbert mixer. The design approach and circuit analysis of the proposed mixer with auxiliary transistors are discussed in section 3. The design realization and simulation results are presented in section 4. A brief conclusion is drawn in section 5.

2 Conventional and Folder Gilbert Mixer Analysis

The conventional Gilbert mixer is shown in Fig. 3. It consists of three stages: trans-conductance stage used for converting voltage to current (V to I converter), switching stage for LO signal and load stage for current to voltage converter (I to V converter). The Gilbert mixer shown in Fig. 3 is a double balanced mixer. The trans-conductance stage consists of source coupled pair transistors M1-M2.

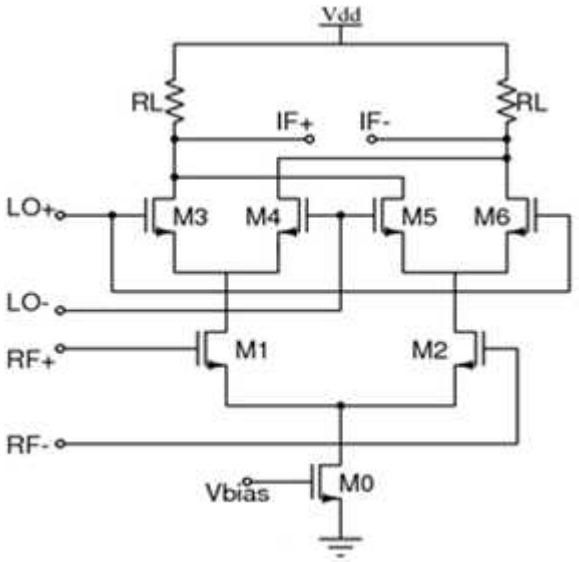

Fig. 3: Conventional Gilbert Mixer

The other SCP's M3-M4 and M5-M6 are used to do switching while load stage converts current to voltage. The analysis of this conventional mixer is presented in table 1. Fig. 4 shows the plot of RF frequency versus Conversion Gain (CG), Noise Figure (NF) and linearity in terms of IIP3. The performance analysis shows that it is necessary to improve all parameters including conversion gain, linearity (IIP3) , noise figure and power dissipation. The conventional mixer is analyzed for linearity i.e. inter-modulation distortion in [3]. As analyzed in [3], the IM3 is given by equation (1).

$$IM3 = \frac{3}{32}\frac{\mu\cos\left(\frac{W}{L}\right)}{I_{ss}}A_{rf}^2 \qquad (1)$$

where: W and L are dimensions of MOS transistor, I_{ss} is the drain saturation current.

Table 1: Performance of Conventional Mixer

Sr. No.	Performance Parameters			
	CG(dB)	NF(dB)	IIP3(dBm)	PD(mW)
1.	9.97	13.19	-3.5	7.8

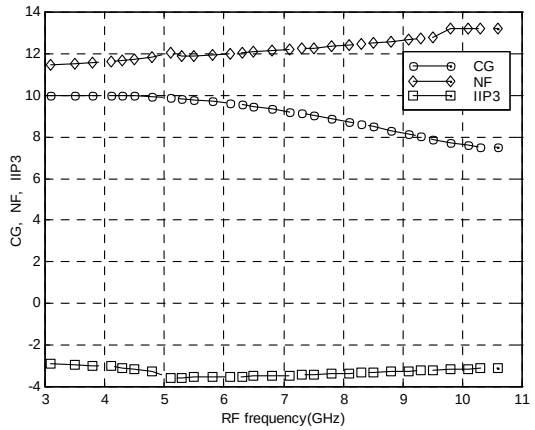

Fig.4: Plot of RF frequency versus CG, NF, IIP3

From equation (1), it can be concluded that to keep distortion low, it is necessary to burn more power and also keep (W/L) ratio or size of transistor down. Both these conditions are undesirable. Thus to design low power mixer with sufficient high linearity, the work in [7] proposes a new topology. In this topology, the folded architecture is used as shown in Fig. 5.

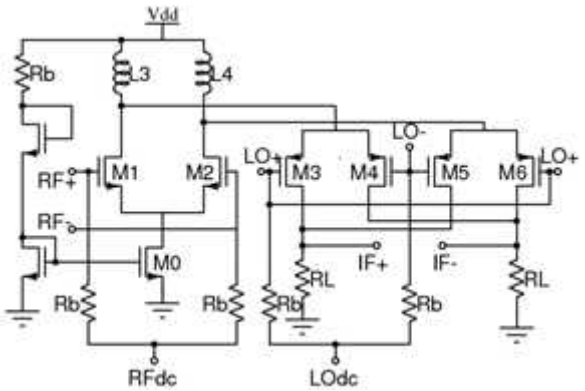

Fig.5: Folded Gilbert Mixer

In the folded mixer topology shown in Fig. 5, the NMOS differential pair M1 and M2 forms the input trans-conductance stage. The PMOS LO switches, M3 through M6 are folded with respect to trans-conductance stage. This technique is effective because PMOS devices with moderate W/L ratio are

sufficiently fast to completely steer the current from trans-conductance stage to LO switches with reasonable LO amplitudes. The bias current through LO switches should be minimize to reduce the flicker noise and DC offset. The V_{gs} of LO switches is set near V_t to achieve a low bias current in LO switches also allows the usage of large load resistance to increase the Conversion Gain (CG) without consuming large IR drop from the limited voltage headroom. The inductors L3 and L4 present high impedance over wide bandwidth of 3.1 to 10.6GHz such that the output AC currents of the trans-conductance stage will flow into LO switches. This folded Gilbert mixer is also analyzed for performance parameters as shown in Table 2.

Table 2: Performance of Folded Gilbert Mixer

Sr. No.	Performance Parameters			
	CG(dB)	NF(dB)	IIP3(dBm)	PD(mW)
1.	14.68	10.62	+5.51	1.4

Fig. 6 shows the plot of RF frequency versus Conversion Gain (CG), Noise Figure (NF) and IIP3.

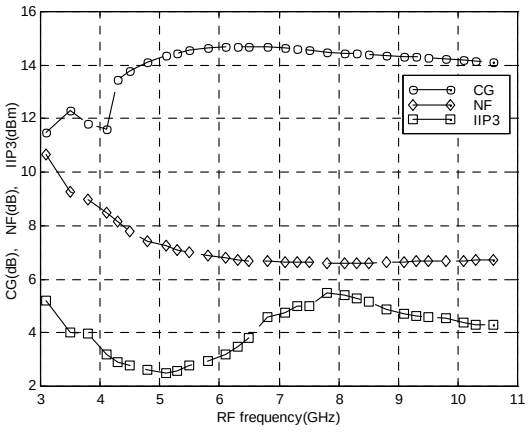

Fig.6: Plot of RF frequency versus CG, NF, IIP3

The performance analysis shows that the conversion gain and power dissipation improves significantly but it is necessary to improve the third order intercept point (IIP3) and noise figure [12] [13]. Gilbert cell mixer linearity depends on the trans-conductance stage. In general, the linearity is represented by the third-order inter-modulation terms. This parameter is measure by applying the third order products from the mixing of RF and LO tones with LO tones at the frequencies given by (2RF±LO)±LO and (2LO±RF)±LO. Generally the most interesting third-order products are: (2RF-LO)-LO and (2LO-RF)-LO as they fall in or close to the IF band.

Several linearization techniques were proposed in [14, 15] to improve the linearity of the mixer. The Multiple Gated Transistor (MGTR) and current-reuse bleeding techniques proposed by [9] and [10] respectively, resulted in high IIP3 but it reduced the conversion gain and consumed more power. The most commonly used technique to improve the linearity is source degeneration. In this source degeneration resistors are added to the trans-conductance stage as shown in Fig. 7.

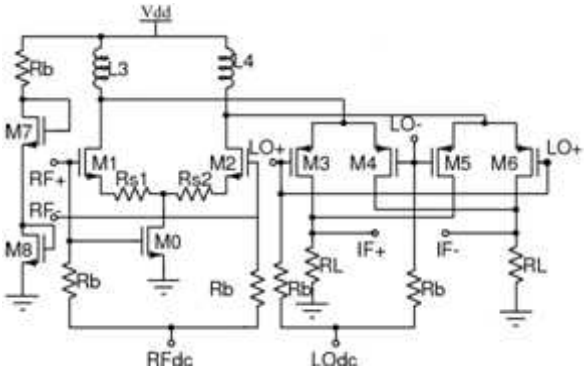

Fig.7: Folded Gilbert Mixer with R_{s1} and R_{s2}

These resistors Rs1 and Rs2 can be adjusted to increase or decrease the linearity or gain. But these resistors will result in degradation of Noise Figure (NF) as they add the thermal noise. Hence instead of resistors Rs1 and Rs2 the source degenerated inductors L1 and L2 are used to increase the linearity without degrading the NF. This Gilbert Mixer with source degenerated inductors L1 and L2 improves the IIP3 to -3dBm, which still can be improved if we add cross-coupled auxiliary transistors M1a and M2a as shown in Fig. 8.

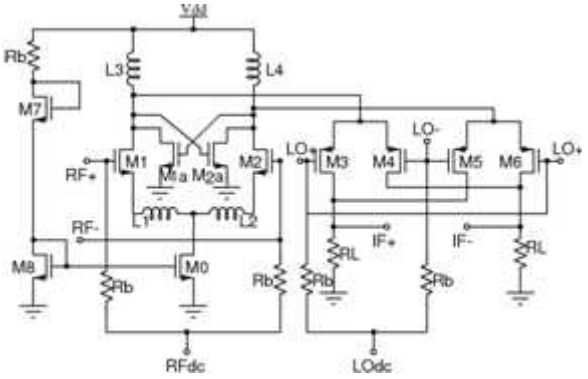

Fig. 8: Complete schematic of proposed mixer

3 Proposed Mixer

Fig. 8 shows the complete circuit diagram of proposed UWB mixer. In this proposed mixer, LO stage is folded with respect to trans-conductance stage to reduce power dissipation and increase conversion gain. It also uses source degenerated inductors L1 and L2 for increasing the linearity and improving NF. Finally the linearity is further increased by using cross-coupled auxiliary transistors M1a and M2a.

The transistors M1 and M2 in trans-conductance stage generates the third-order inter-modulation terms which degrades the linearity of conventional mixer. If the third-order inter-modulation terms IM3 are cancelled or removed after the post generation, then the linearity of conventional mixer can be improved. The auxiliary transistors M1a and M2a, called cross-coupled pairs, are biased in weak inversion. These transistor generate non-linear current required to cancel the third order inter-modulation terms IM3 generated by M1 and M2. The basic operating principle of this technique can be explained by assuming that all devices are perfectly matched and ignoring the reactive components. Referring the Fig. 9, the drain current of each transistor can be represented as a power-series expression.

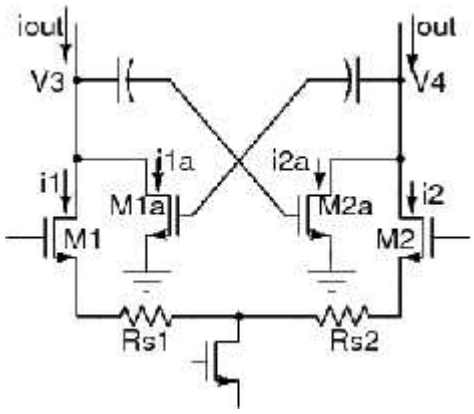

Fig. 9: Cross section of mixer showing auxiliary transistor

$$i_1 = g_1 v_1 + g_2 v_1^2 + g_3 v_1^3 \quad (2)$$

$$i_{1a} = g_{a1} v_4 + g_{a2} v_4^2 + g_{a3} v_4^3 \quad (3)$$

$$i_2 = -g_1 v_1 + g_2 v_1^2 - g_3 v_1^3 \quad (4)$$

$$v_4 = -i_2 R_{on} = a v_1 + b v_1^2 + c v_1^3 \quad (5)$$

where R_{on} is the switch-on resistance of the switch pair.

$$a = R_{on} g_1 , \qquad b = R_{on} g_2 , \qquad c = R_{on} g_3$$

The two nonlinear currents i_1 and i_{1a} adds at node v_3, yielding output current i_{out}^+. (Ref. Fig. 9).

$$i_{out}^+ = i_1 + i_{1a}$$

$$= (g_1 + a g_{a1}) v_1 + (g_2 a^2 g_{a2} + b g_{a1}) v_1^2 +$$

$$(g_2 + c g_{a1} + 2ab g_{a2} + a^3 g_{a3}) v_1^3 \quad (6)$$

The coefficient g_3 of the third order term v_1^3 in equation (2) is a dominant source of third order inter-modulation distortion, which limits the linearity of a mixer. To improve the linearity, g_3 should be minimized without reducing the fundamental trans-conductance g_1. The transistor pair M1 and M2 in the trans-conductance stage is biased in strong inversion and hence has negative third-order g_3 in the equation (2). Therefore, the auxiliary cross-coupled transistor M1a and M2a are biased in weak inversion thereby producing positive third-order terms g_{a3} and g_{a2}, which cancels the negative third-order term g_3. From equation (6), it can be observed that the current i_{1a} partially cancels both the second and third order terms of current i_1.

Fig. 10 shows the small-signal equivalent circuit of proposed mixer used for distortion analysis.

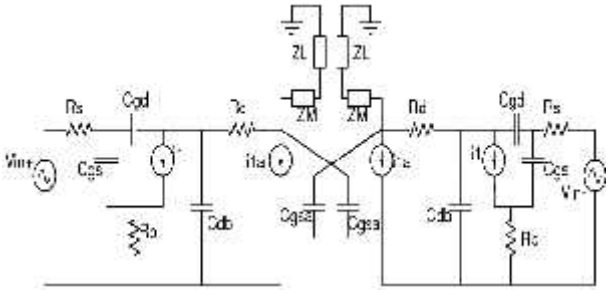

Fig. 10: Small signal equivalent circuit of proposed mixer

Except the gate-source capacitance, the parasitic capacitance and resistance of two-auxiliary transistors have been neglected in the analysis. A time varying Volterra series analysis can be used to analyze the inter-modulation performance of the proposed mixer. The detail analysis of the distortion

using Volterra series analysis is provided in [11] and is given by equation (7).

$$IIP_3 = \frac{1}{6R_s|H(\omega)||A_1|.2.|\epsilon(\Delta\omega_1 + \Delta\omega_2)|} \quad (7)$$

Where:

$$H(\omega) = \frac{1 + j\omega C_{gs}(R_s + R_p) + j\omega C_{gd}R_s}{g_1 - j\omega C_{gd}[1 + R_p(g_1 + j\omega C_{gs})]} \quad (8)$$

$$A_1(\omega) = \frac{1}{g_1 + g(\omega)} \frac{1 + j\omega C_{gd}Z_1(\omega)}{Z_2(\omega)} \quad (9)$$

$$\epsilon(\Delta\omega, \omega_1 + \omega_2) = g_3 - g_{oB} \quad (10)$$

$$g_1' = g_1 - ag_a \quad (11)$$

$$g_3' = g_3 - cg_{a1} - 2abg_{a2} - a^3g_{a3} \quad (12)$$

$$g_{oB} = \frac{2(g_2')^2}{3}\left[\frac{2}{g_1' + g(\Delta\omega)} + \frac{1}{g_1' + g(\omega_1 + \omega_2}\right] \quad (13)$$

$$g_2' = g_2 + bg_{a1} + a^2g_{a2} \quad (14)$$

$$g(\omega) = \frac{1 + j\omega C_{gd}[R_s + Z_1(\omega)] + j\omega C_{gs}[R_s + Z_2(\omega)]}{Z_2(\omega)} \quad (15)$$

$$Z_1(\omega) = \frac{1}{j\omega C_{db}} || \left\{\left[(Z_N + Z_L)|| \frac{1}{j\omega C_{gsa}}\right] + R_d\right. \quad (16)$$

Where:

Z_N = the equivalent impedance of switch transistors

Z_L = the equivalent impedance of load

$Z_2(\omega) = R_p + j\omega C_{gd}[R_sR_p + R_sZ_L(\omega) + R_pZ_L(\omega)$

In the above equations, the g_{oB} is the combined effect of second order inter-modulation terms, which then mixed with fundamental tones, yielding the third-order products [11]. This self-interaction is due to the multiple feedbacks in the circuit mainly by the gate-drain capacitance [11].

4 Simulation Results

The proposed folded Gilbert mixer with inductive source degeneration and CCPDT was designed and simulated using UMC 65nm CMOS process. All the simulations were done at 0.8V supply voltage and the total power dissipation is 3.6mW including bias circuit. The conversion gain of the proposed mixer was measured for an IF frequency of 10MHz with both RF and LO ports swept in frequency up to 11GHz. The RF and LO signal powers were set to be -30dBm and 2dBm respectively.

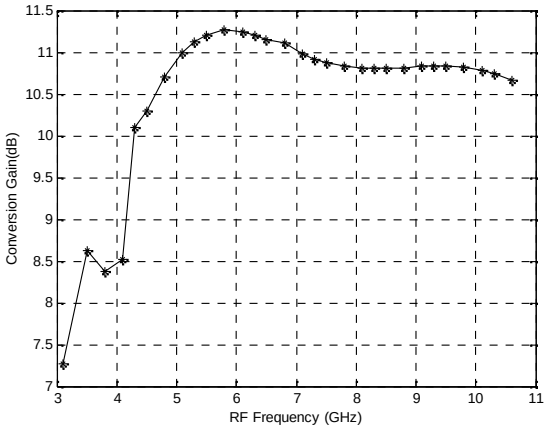

Fig.11: CG versus RF frequency

The simulated conversion gain versus RF frequency is shown in Fig. 11. The mixer achieved a conversion gain of better than 7.27dB over a wide frequency from 3.1GHz to 10.6GHz. The conversion gain also exhibited a 3-dB variation across the RF frequency of 3.1GHz to 10.6GHz with an average conversion gain of 8dB and maximum gain of 11.27dB.

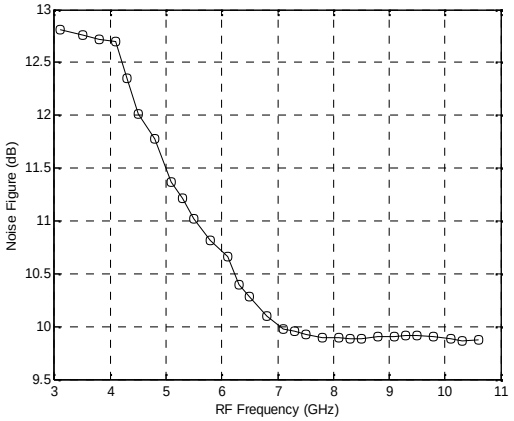

Fig.12: DSB NF versus RF frequency

Fig. 12 shows the double side band (DSB) Noise Figure (NF) as function of RF frequency. The proposed mixer exhibited DSB NF of 10.4dB. In fig. 13, it is seen that the RF input 1-dB compression point (IP1-dB) of -3.62dB is obtained. Fig. 14 depicts the main signal power and third-order inter-modulation power as function of the RF input power. There are two signals fed to the RF input port for IIP3 measurement, one at 8.011GHz and other at 8.01GHz.

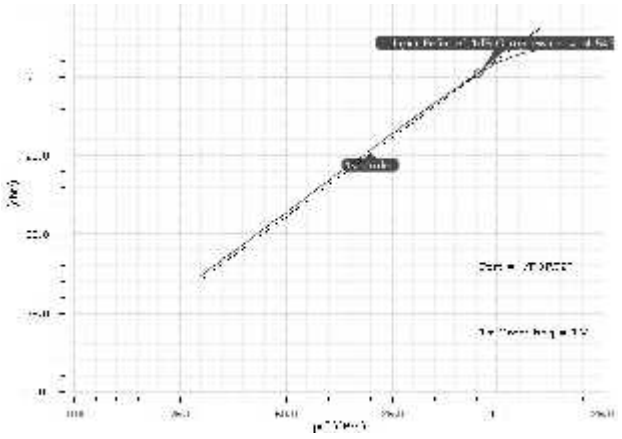

Fig. 13: 1-dB compression point

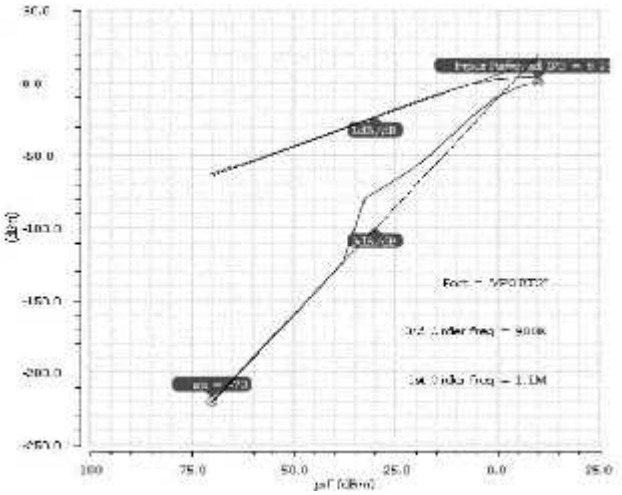

Fig. 14: IIP3 of Proposed Mixer

The LO signal has frequency of 8GHz and power level of 2dBm. The proposed mixer exhibited an input third-order intercept point (IIP3) of +8.25dBm at RF frequency of 8GHz. Finally, IP1-dB and IIP3 were measured for various RF frequencies ranging from 3.1GHz to 10.6GHz. The results are shown in figure 13. In the simulation measurement, the LO power was set as 2dBm and the IF frequency was fixed at 10MHz. Table 3 shows the comparison of conventional Gilbert mixer, folded Gilbert mixer and proposed folded Gilbert mixer with inductive source degeneration and CCPDT. The comparison shows that the folded Gilbert mixer exhibits an excellent conversion gain of 14.6dB while consuming only 1.4mW with low supply voltage of 0.8V.

Table 3: Comparison of UWB Mixers

Sr. No.	Types/ Parameters	Conventional Gilbert Mixer	Folded Gilbert Mixer	Proposed Folded Gilbert Mixer with CCPDT
1.	CG(dB)	9.97-7.4	11.4-14.6	7.27-11.27
2.	NF(dB)	11.47-13.2	10.65-6.72	9.87-12.7
3.	IIP3 (dBm)	-3.2@ 8.5GHz	+5.51@ 8.5GHz	+8.6 @8.5GHz
4.	PD (mW)	7.8mW at 1.2V	1.4mW at 0.8V	3.6mW at 0.8V

It has reasonably good IIP3 of +5.51dBm. Whereas the proposed mixer has excellent IIP3 of +8.6dBm with reasonably good conversion gain of 10.92dB while consuming 3.6mW. Thus adding two cross-coupled auxiliary transistor and inductive source degeneration in folded Gilbert mixer is justified as it improves the IIP3 by 3.1dBm while slightly reducing the conversion gain which is acceptable if used in UWB receiver front-end. The proposed mixer is compared with state-of-art Gilbert cell mixers [4]-[8] in the table 4.

5. Conclusion

In this paper, a fully optimized UWB mixer for CG, IIP3, NF and power consumption using 65nm CMOS technology has been presented. The folded approach was applied to reduce supply voltage and dc power consumption. The CCPDT improves the IIP3 drastically while giving acceptable CG and NF which is suitable for applications in receiver front-end for various wireless communication systems specially UWB systems

Table 4: Performance comparison of this work with present work

Reference	This Work	[4]	[5]	[6]	[7]	[8]
Frequency(GHz)	3.1 – 10.6	1.9	1.9	1.9	3 - 7	2 - 11
Process	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	0.13um CMOS	0.18um CMOS
Vdd	0.8V	1.2V	1.2V	1.2V	0.8V	1.8V
CG (dB)	11.27	8.75	13.97	12.42	8.2	6.9
NF (dB)	12.7	4.12	3.13	8.92	13.5	15.5
IIP3 (dBm)	+8.6	+11.6	+1.7	+6	-3.2	6.5
IP1-dB (dBm)	-4.25				--	-3.5
LO Power(dBm)	+2					-5
P.D. (mW)	3.6	2.17	2.02	2.02	2.5	25.7

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