Design and Implementation of Digital Butterworth IIR filter using Xilinx System Generator for noise reduction in ECG Signal

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Abstract: Application Specific Integrated Circuits (ASICs) and Digital Signal Processors are generally used for implementing digital filters. Now days in the advances in technology leads to use of field programmable Gate Array (FPGA) for the implementation of Digital Filters. The Present paper deals with Design and implementation of digital IIR Butterworth filter using Xilinx System Generator. The Quantization and Overflow are main crucial parameters while designing the filter on FPGA and that need to be consider for getting the stability of the filter. As compare to the conventional DSP the speed of the system is increased by implementation on FPGA. Digital Butterworth filter first designed analytically for the desired Specifications and simulated using Simulink in Matlab environment. This paper also proposes the method to implement Digital IIR Butterworth Filter by using Xilinx system generator. The filer has shown good performance for noise removal in ECG Signal.

Key–Words: Xilinx System Generator, Butterworth Filter, noise Reduction.

1 Introduction

IIR filters are widely used for lower sampled rates. These filters are supported in terms of IP cores, software and Tools. To ensure satisfactory operations many times it is necessary to evaluate the various parameters like Overflow, stability and quantization like internal quantization, coefficient Quantization [1]. In this paper the digital Butterworth IIR filter is simulated and its performance is studied for high frequency noise removal from ECG signal. Harish V. Dixit et.al [4] have implemented IIR filter using Xilinx system generator. They showed that the computational capability is increased in implementation of IIR filter. For getting simulation model Simulink is used. Due to some quantization error filter has goven some sort of instability. Anurag Agarwal et.al have designed FIR filter using windows on System generator [5] In this signal used is music signal and gives best results for Blackmans window. Kumudini Sahu et.al, have implemented a structure for FIR filter with 19 taps and input signals contaminated with noise. Filter has proved to have good response for adaptive noise cancellation [6-8]. Ayesha Firdous and B.Rajan have used Xilinx power estimator to estimate the power consumption of FPGA [9]. Emmanuel S. Kolawole et.al [11] have implemented Low-Pass, High-Pass and Band-Pass Finite Impulse Response (FIR) Filters Using FPGA. The synthesis report shows that there is increase in speed of computation; les resource usage, highly flexible, power efficient and low cost and it proved the parallelism nature of FPGA Sushmitha.C et.al proposed paper with multipliers, in which multipliers outweigh adders in cost. Therefore they highlighted the need of other type of profitable multipliers. S. Mirzaei et.al they have presented method for implementation of high speed FIR filter using registers and hardwired shifts. They have used modified common sub-expression elimination algorithm. Sweety Kashyap et.al have Implemented FIR Filter of High Performance Using Low Power Multiplier and Adder [14]. This paper highlights the implementation of IIR filter using MATLAB Simulink model and Xilinx system generator blocks for high frequency noise reduction in ECG signal.

1.1 Digital Filter Information

The digital filter information is given below in tabular form, the table 1 describes the detail information of Butterworth filter used for design, and whereas table 2 shows filter specifications used during implementation of filter, table 3 shows actual implementation cost in terms of number of components such as multipliers and adders used.

Table 1: Butterworth Filter Information

Filter structure	Direct form II
Number of sections	1
Filter Stability	Stable
Linear Phase	No
Design algorithm	Butter

Table 2: Filter Design Specifications

Sampling frequency Fs	1000Hz
Filter response	Low pass
Filter order	2
Fcutoff	.2
3dB point	0.2
6dB Point	0.25725

1.2 Design Scheme

As important information in the ECG signal lies in the frequency range of .05Hz to 100Hz.[2] it is decided to design a low pass filter of cutoff frequency 100Hz to remove high frequency noise signal. Butterworth filter gives flat response in the pass band. Sampling frequency used in the design of filter is 1000Hz.

1.3 Realization of Filter

The figure 1 shows design of Butterworth filter using FDA Tool whereas figure 2 shows realization model of the filter.

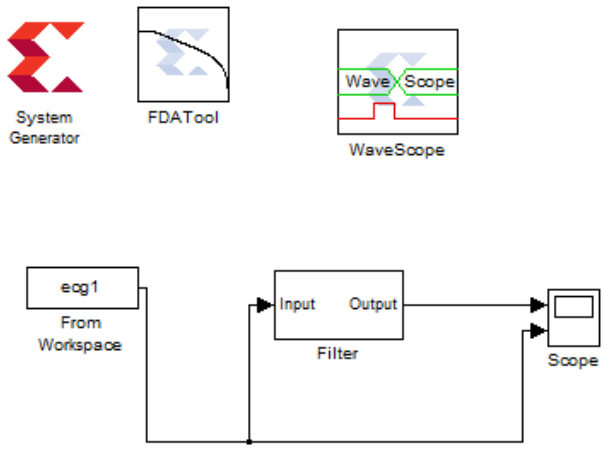

Figure 1: Design of IIR Butterworth filter using FDA tool

Table 3: Filter Implementation Cost

Number of Multipliers	4
Number of adders	4
Number of states	2
Multiplication per input sample	4
Addition per input sample	4

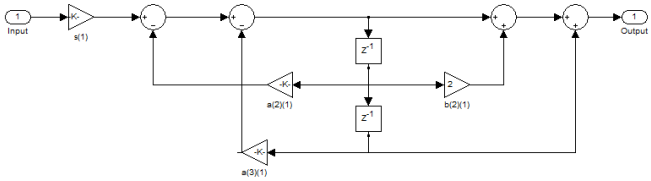

Figure 2: Realization model of IIR Butterworth Low pass filter using FDA Tool.

1.4 Implementation Steps:

For the implementation of the Butterworth digital filter following implementation steps are followed. The implementation steps are as follows.
Step 1: Design of low pass filter using FDA Tool.
Step 2: Create Simulink Model using Xilinx System Generator.
Step 3: Identify the Filter Coefficients.
Step 4: Complete the simulation model using Xilinx basic elements (Xilinx system generator block is compulsory)
Step 5: Execute the model ad observe the waveform on Scope.
Step 6: Get Detail summary report which includes the device utilization, Time and power analysis.
Step 7: Get RTL Schematic of the Designed filter
The figure 3 shows design of Butterworth filter designed and implemented using Xilinx System generator basic block set. The details of the filter design along with the results n filter frequency responses are explored which are discussed further.

1.5 Filter coefficients

Numerator: 1, 2, 1
Denominator: 1, -1.142, 0.4128
Gain: 0.0674
Output Gain: 1
Transfer function of Low pass Butterworth filter

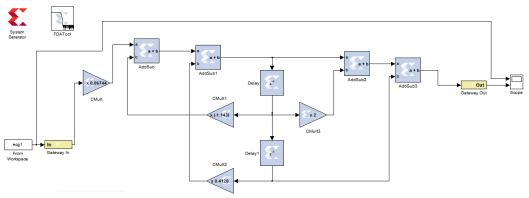

Figure 3: IIR Butterworth Low pass filter using Xilinx System Generator

$$H(z) = \frac{0.067(1 + 2z^{-}1z^{-}2)}{(1 - 1.142z^{-}1 + 0.4162z^{-}2} \qquad (1)$$

1.6 Filter Responses

The various responses are depicted in figure 4 to figure 11. These response shows that designed filter having flat response in pass band and is stable with nonlinear characteristics.

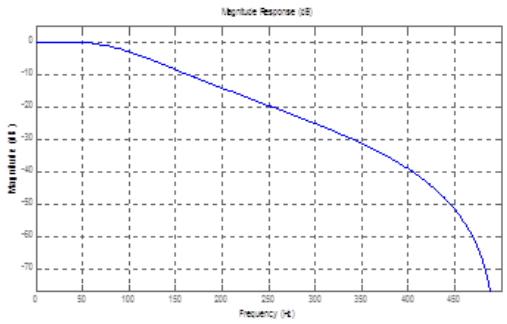

Figure 4: Magnitude response

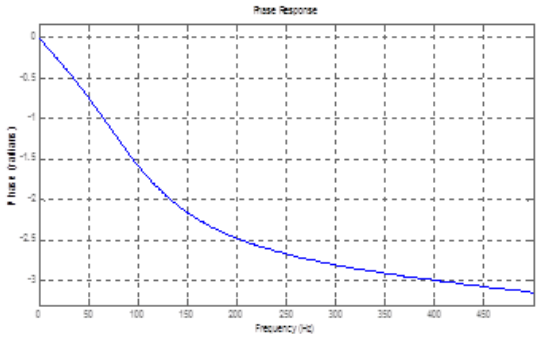

Figure 5: Phase Response

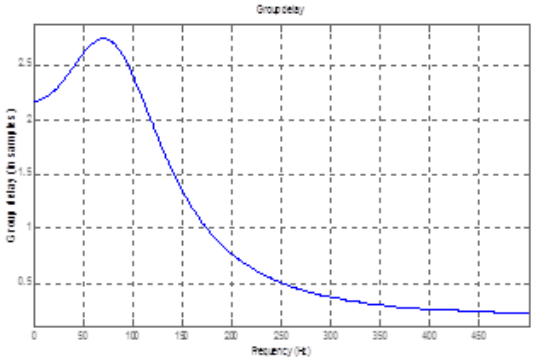

Figure 6: Group Delay

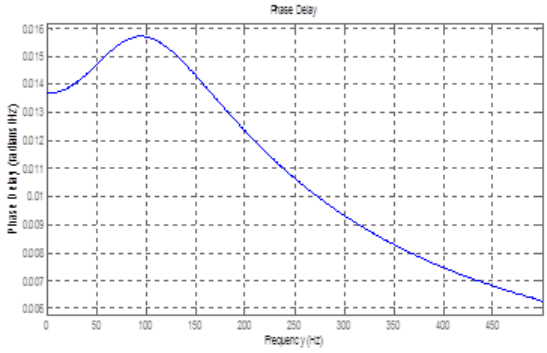

Figure 7: Phase Delay response

2 Implementation Results

In this filter ECG Signal is applied with high freq noise, the following figure shows input output waveforms before and after filtration where noise above 100 Hz is filtered.Figure 12 shows the output of the filer

2.1 Device Utilization Summary

Following table gives the utilization summary of the designed system

Table 4: Device utilization summary

Logic Utilization	Available	Used	Utilization
Number of Slice Flip Flops	9312	4	1 Percent
Number of 4 input LUTs	9312	23	1 Percent
Number of occupied Slices	4656	40	1 percent
Slices containing related logic	40	40	100
Total Number of 4 input LUTs	9,312	72	1
Fanout of Non-Clock Nets		1.04	

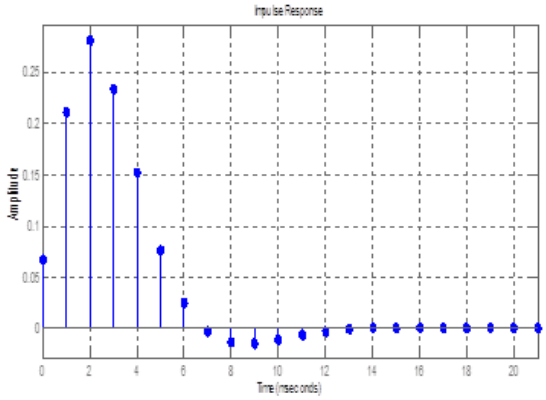

Figure 8: Impulse response

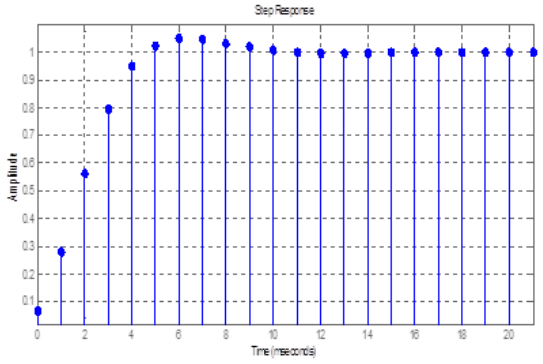

Figure 9: Step response

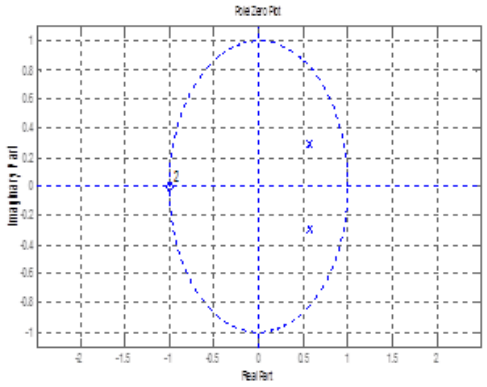

Figure 10: pole zero Diagram

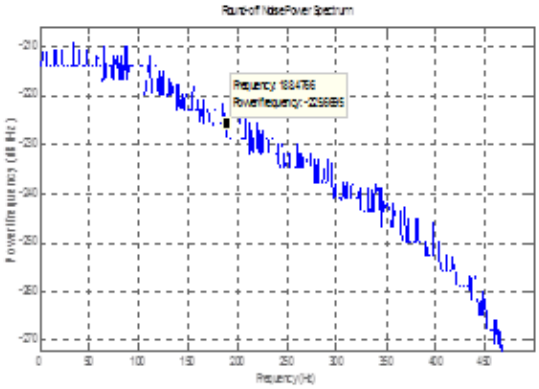

Figure 11: Round Off Noise power Spectrum

2.2 RTL Schematic

Figure 13 and Figure 14 shows the RTL Schematic of the proposed filter.

3 Conclusion

In the paper low pass Butterworth filter is designed and implemented for noise reduction in ECG signal on Xilinx platform. Filer is implemented for order 2. Filter has shown good performance in terms of area, power and Speed when used on FPGA platform. Filter designed have shown good filtering response for reducing high frequency noise from ECG signal.

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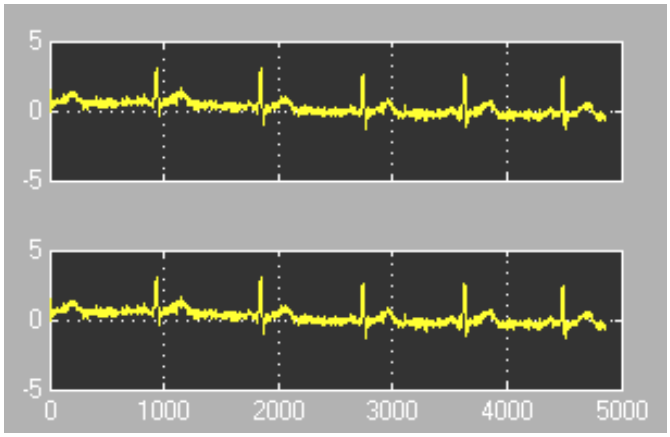

Figure 12: Input Output waveforms of digital filter

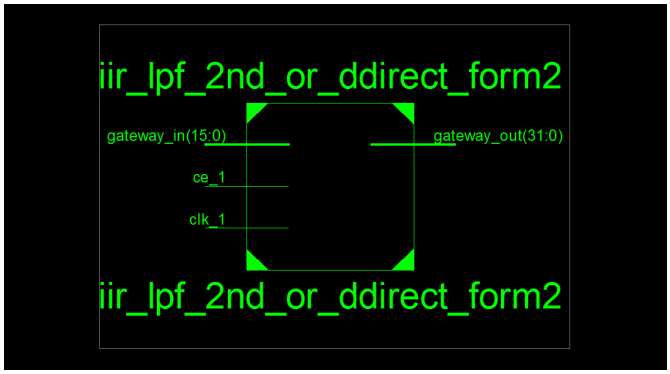

Figure 13: RTL Schematic 1

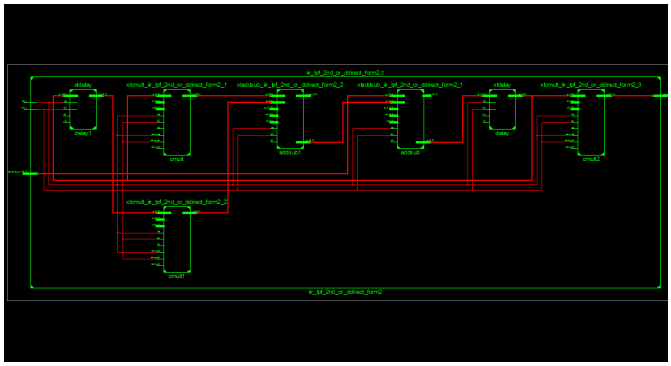

Figure 14: RTL Schematic 2

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