Revolt a Performance of IMD by Rectified Number of MLI Through Simulink Computational Method

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Abstract: Titled research work has been dealt with three different topologies of Multilevel Inverter. In the past decades, the researchers have dealt with the conventional topology one which possesses the twelve switches of Multilevel Inverter is applied to an Induction motor drive. The present research work has been introduced a new topology II system which reduces 10 and 5 switches in induction motor. The performance of the research work has been investigated through MATLAB simulation.

Keywords: Conventional Topology; Multilevel Inverter; Total Harmonics Distortion.

1. Introduction

Nowadays, multilevel inverters have received more attention for their ability on high power and medium voltage operation and for other advantages such as high power quality, low order harmonics, lower switching losses and better electromagnetic interferences [1] These cascaded multilevel inverter generate a stepped voltage waveform, and more number of dc voltage waveform and switches will be used and they explain only the inverter operation and do not explain in application oriented. [2] These multilevel inverter are using a single phase seven level inverter for grid connected system. They are not implemented in induction motor, These cascaded h-bridge multilevel inverter generate a stepped waveform and more number of switches will be used and they explain only the single phase operation of multilevel inverter. They are not implemented in induction motor. [3] These symmetric multilevel inverter introduce the least number of switches, and gate trigger circuitry, switching loss are reduced, cost and size, but it is implemented in single phase circuit. [4] These cascaded multilevel inverter are using a nine and seven switches and sinusoidal pulse with modulation (SPWM) technique is also implemented using multicarrier wave signals, but they are not used in three phase circuit and used only in induction motor drive.[5]; [6]; [7]; [8];[9];[10]; [11]In recent years, different symmetric cascaded multilevel inverters have been presented, the main disadvantage of these circuits is some of them use a high number of bidirectional switches. More number of insulated gate bipolar transistors is required and they are not implemented in three phase circuit and induction motor drive.

Generally, voltage source inverter (VSI) and current sources inverter (CSI) are widely used for grid integration of renewable energy; recent trend goes towards the use of multilevel inverter. Because of these several benefits, MLI generates output having less distortion, produces lesser common mode voltage, produces less stress, reduces electromagnetic interference and generates better quality output.MLI also pertains to lesser and smaller filter size[12];[13].Several commercial MLI topologies are existing such as neutral point clamped inverter, flying capacitor, cascaded H bridge Among these, cascaded multilevel inverter is suited for induction motor drives application. In this paper, a new topology of multilevel inverter is proposed in order to increase the number of output voltage levels and reduce the number of switches, drives circuit, total cost of the inverter, and implementation of three phase circuit and induction motor drives. Moreover, the proposed topology is compared with other topologies from the different point of view. Such as number of IGBT, number of dc sources and performances of induction motor drives. Finally, the performances of the proposed topology in generating are voltage levels through a seven levels inverter is confirmed by simulation using a (MATLAB/SIMULINK).

2. Conventional Method

2.1 A 12 Switches Cascaded H-Bridge topology.

A single-phase structure of an m-level cascaded inverter is illustrated in Fig.1 . Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by $m = 2s + 1$, where s is the number of separate dc sources. A stepped output voltage and current can be obtained in a cascaded MLI by cascading several H-bridge inverters. Adding another H-bridge to the existing H-bridge, number of levels increases by two. Hence for a 7-level output, three H-bridge inverters are to be cascaded as shown in Fig. 2. The switching states of the cascaded 7- level multilevel inverter are shown in Table1.Simulation results of output voltage waveform, THD and performance curve of induction motor and the content of conventional cascaded 7- level multilevel inverter respectively are shown in Fig.(3,4&5).

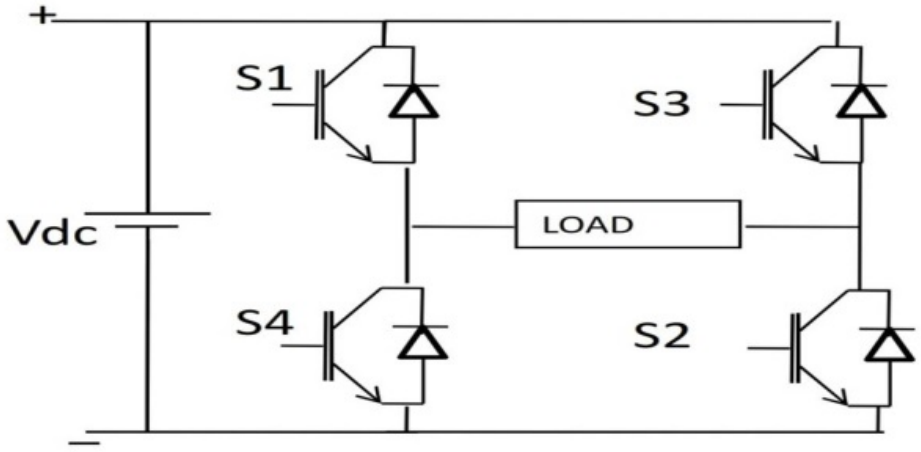

Fig:1 A single-phase structure of an m-level cascaded inverter

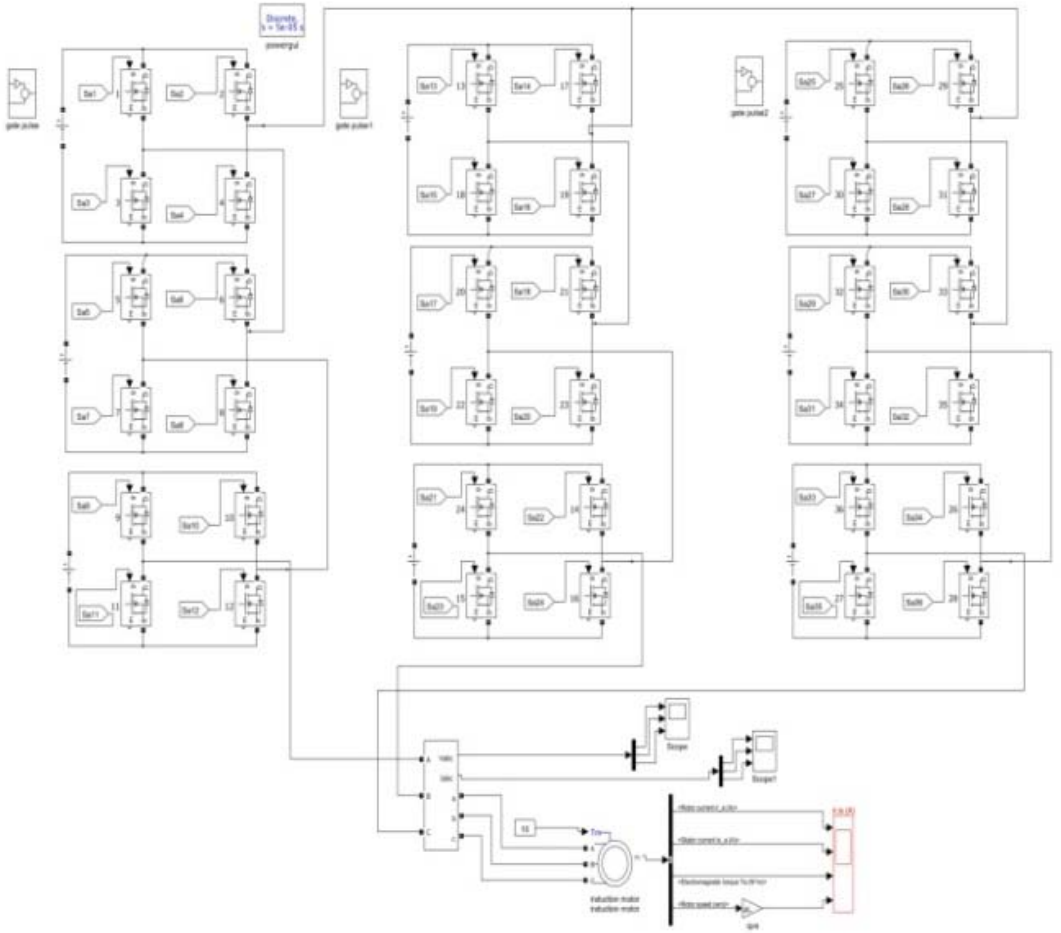

Fig2: Three phase cascaded multilevel inverter

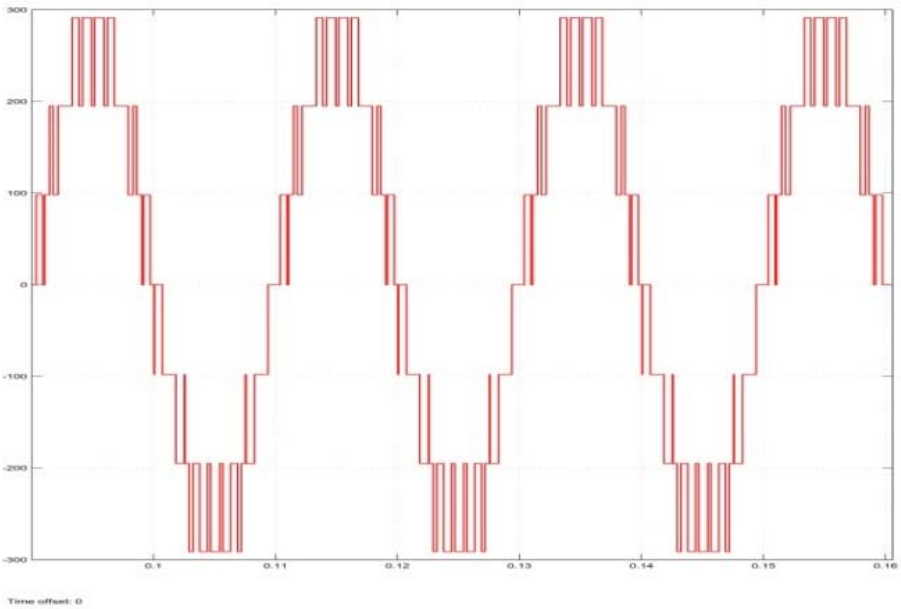

Fig3: Output voltage of seven level inverter

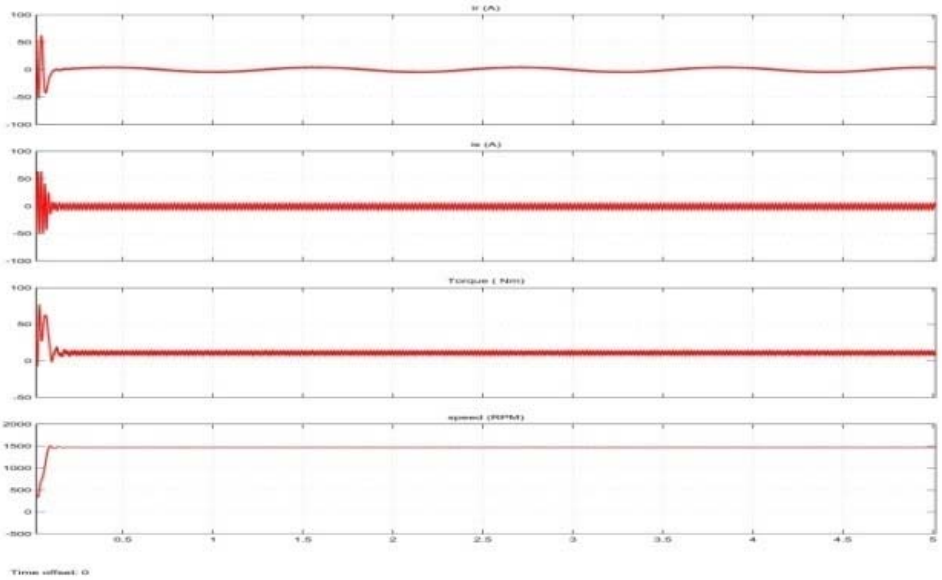

Fig4: Performance of induction motor drive

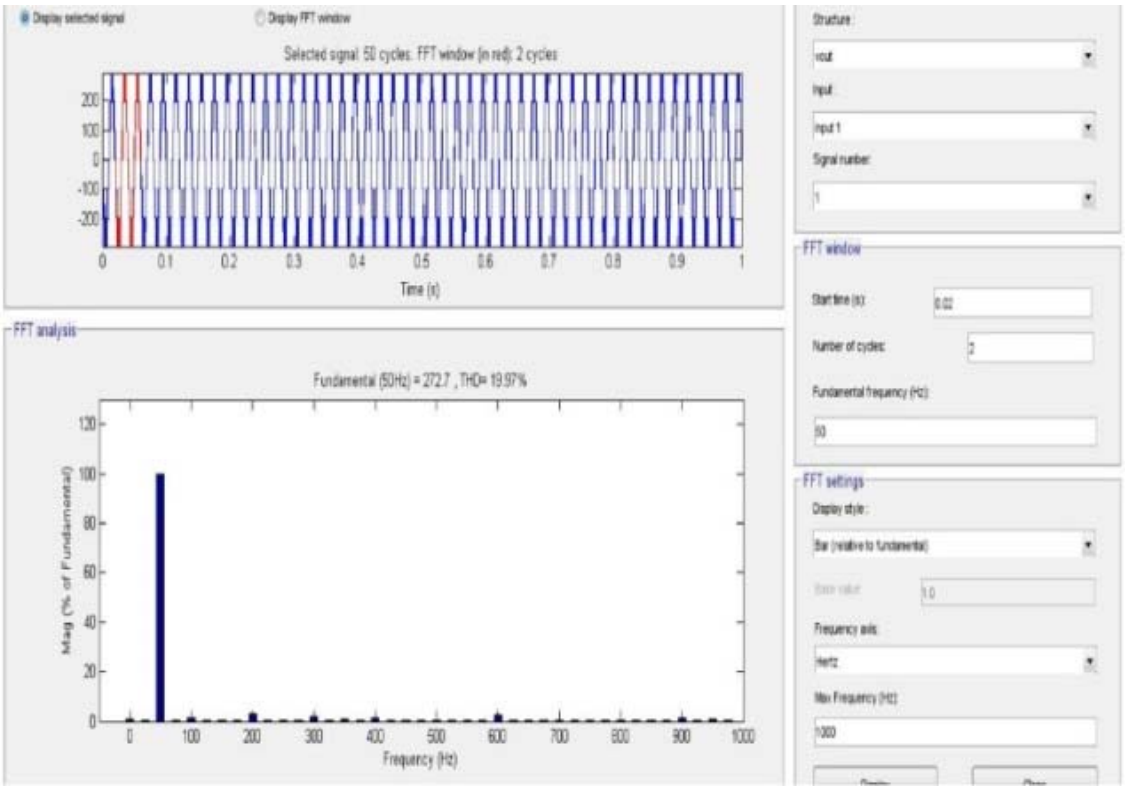

Fig5: FFT spectrum of seven level inverter

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
V_{dc}	1	0	0	1	0	0	1	1	0	0	1	1
$2V_{dc}$	1	0	0	1	0	0	1	1	1	0	0	1
$3V_{dc}$	1	0	0	1	1	0	0	1	1	0	0	1
$0V_{dc}$	1	0	1	0	1	0	1	0	1	0	1	0
$-V_{dc}$	0	1	1	0	1	1	0	0	1	1	0	0
$-2V_{dc}$	0	1	1	0	0	1	1	0	1	1	0	0
$-3V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0

Table1: Switching sequence of cascaded multilevel inverter using 12 switches

3. Induction motor model

The dynamic model of an induction motor in the stationary reference frame can be written in d-q frame variables. Stator voltage Vector V_s of the motor can be expressed as follows:

$$\mathrm{Vds} = \left(\mathrm{d}\psi * \frac{\mathrm{ds}}{\mathrm{dt}}\right) + (\mathrm{Rs} * \mathrm{Ids}) \quad (1)$$

$$\mathrm{Vqs} = \left(\mathrm{d}\psi * \frac{\mathrm{ds}}{\mathrm{dt}}\right) + (\mathrm{Rs} * \mathrm{Iqs}) \quad (2)$$

$$\psi\mathrm{s} = \left(\mathrm{d}\frac{\psi\mathrm{s}}{\mathrm{dt}}\right) + (\mathrm{Rs} * \mathrm{Is}) \quad (3)$$

The stator flux vector ψs and components can be written as:

$$\Psi\mathrm{ds} = \mathrm{Ls} * \mathrm{Ids} + \mathrm{Lm} * \mathrm{Idr} \quad (4)$$

$$\Psi\mathrm{qs} = \mathrm{Ls} * \mathrm{Iqs} + \mathrm{Lm} * \mathrm{Iqr} \quad (5)$$

$$\Psi s = Ls * Is + Lm * Ir \quad (6)$$

The rotor flux vector ψr and components in the stator reference frame is

$$\psi\mathrm{dr} = \mathrm{Lr} * \mathrm{Idr} + \mathrm{Lm} * \mathrm{Ids} \quad (7)$$

$$\psi\mathrm{qr} = \mathrm{Lr} * \mathrm{Iqr} + \mathrm{Lm} * \mathrm{Iqs} \quad (8)$$

$$\psi\mathrm{r} = \mathrm{Lr} * \mathrm{Ir} + \mathrm{Lm} * \mathrm{Is} \quad (9)$$

where Vds and Vqs are the stator voltages; Ids and Iqs are the stator currents; Idr and Iqr are the rotor currents; Ψds and Ψqs are the stator fluxes; ψdr and ψqr are the rotor fluxes; Is and Ir are the stator and rotor currents vectors; Rs is the stator winding resistance., and Ls , Lr, Lm are stator, rotor self inductance and mutual inductance respectively. The electromagnetic torque Te is developed by the induction motor in terms of stator and rotor flux vectors *can* be expressed as:

$$\mathrm{Te} = 3/2 * \mathrm{p}(\mathrm{Lm}/\sigma\mathrm{LsLr})\ \psi\mathrm{s} * \psi\mathrm{r}$$

$$\mathrm{Te} = 3/2 * \mathrm{p}(\mathrm{Lm}/\sigma\mathrm{LsLr})\ |\psi\mathrm{s}| * |\psi\mathrm{r}| \sin(\delta) \quad (10)$$

Where $\sigma = 1 - (\mathrm{Lm\^{}2}/\mathrm{Ls} * \mathrm{Lr})$ is the leakage factor; p is the number of pole pairs and δ is the torque angle. From the above equation, it is clear that the electromagnetic torque is cross vector product between the stator and rotor flux vectors. Therefore, generally torque control can be performed by controlling torque angle δ with constant amplitude of the stator and rotor fluxes.

4. A 10 Switches multilevel inverter topology

In conventional multilevel inverter, both positive and negative polarities in power switches are operated to produce a high frequency waveform. There is no need to use the switches to attain bipolar level. This basic structure of new proposed topology is shown in Fig 6. The power semiconductor switches in generation level is employed for polarity generation operating at the line frequency. The switching order for the generation of positive levels (0, $V_{dc}/3$, $2V_{dc}/3$, V_{dc}) are shown in Table 2. The required output voltage levels produced by the level generator are generated as follows; switches S_2, S_4, S_6 are ON which short circuit the input terminal AB of the polarity generation resulting in the generation of the zero. The current path that is active at this stage in zero output level. In one third positive output level, Switching S_2, S_4, S_5 are ON by connecting the terminal a to $V_{dc}/3$ and terminal B to ground resulting in the generation of V_{dc} at all other high frequency controlled switches. Switches S_2, S_3 are ON and connecting the terminal A to $2V_{dc}/3$ formed by the sum of two equal capacitor voltages and terminal B to ground in two-third positive output voltage. In maximum positive output level, S_1 is ON and terminal A is connected to V_{dc} and terminal B is ground resulting in generation of V_{dc} .In forward mode: switches S_7&S_8 are ON, generating the positive polarity output. In reverse mode: switches S_9 & S_{10} are ON, generating the negative polarity output. The gate pulse for MLI is shown in Fig.7& 8 respectively. The output voltage waveform & performance curve of induction motor are shown in Fig 9&10 respectively and the total

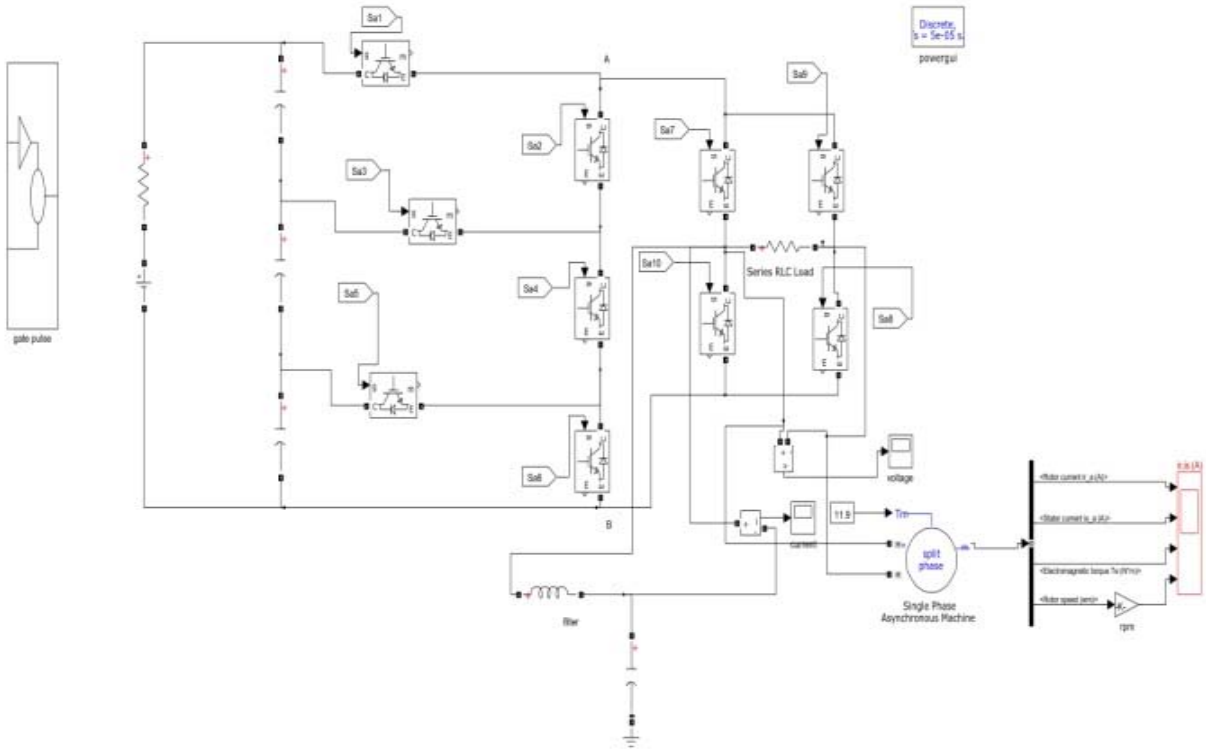

Fig6: Three phase Multilevel inverter using 10 switches

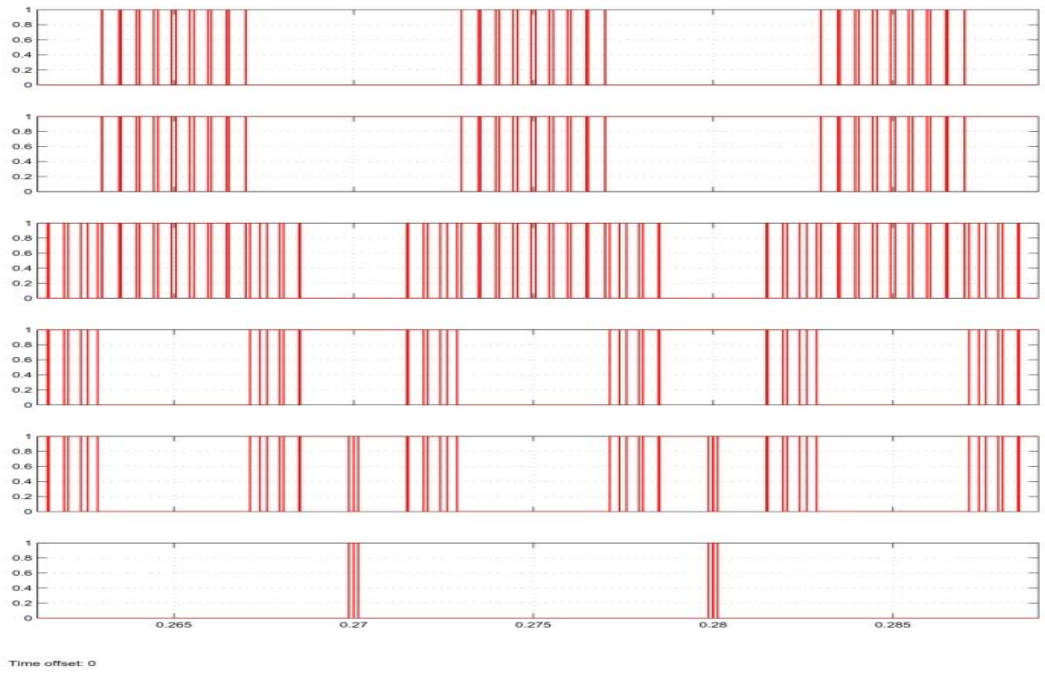

Fig7: Gate pulse of Multilevel inverter using 10 switches

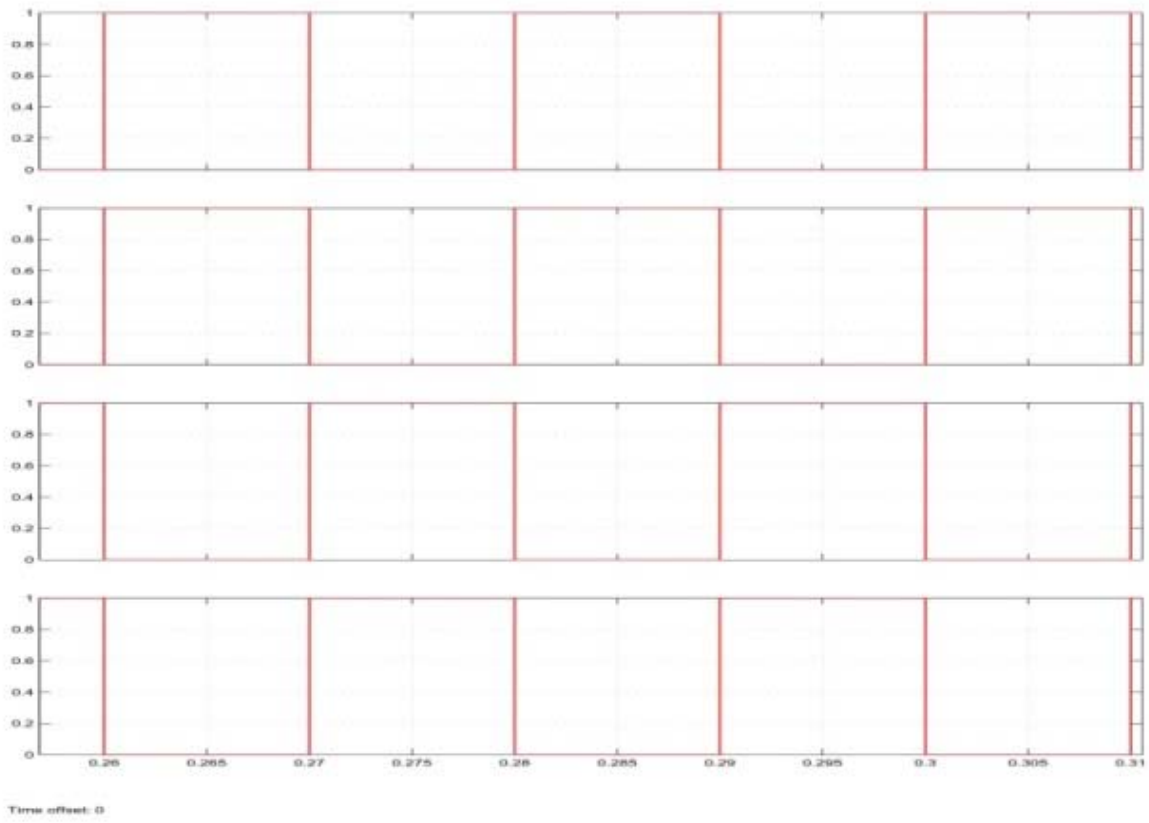

Fig8: gate pulse of Multilevel inverter using 10 switches

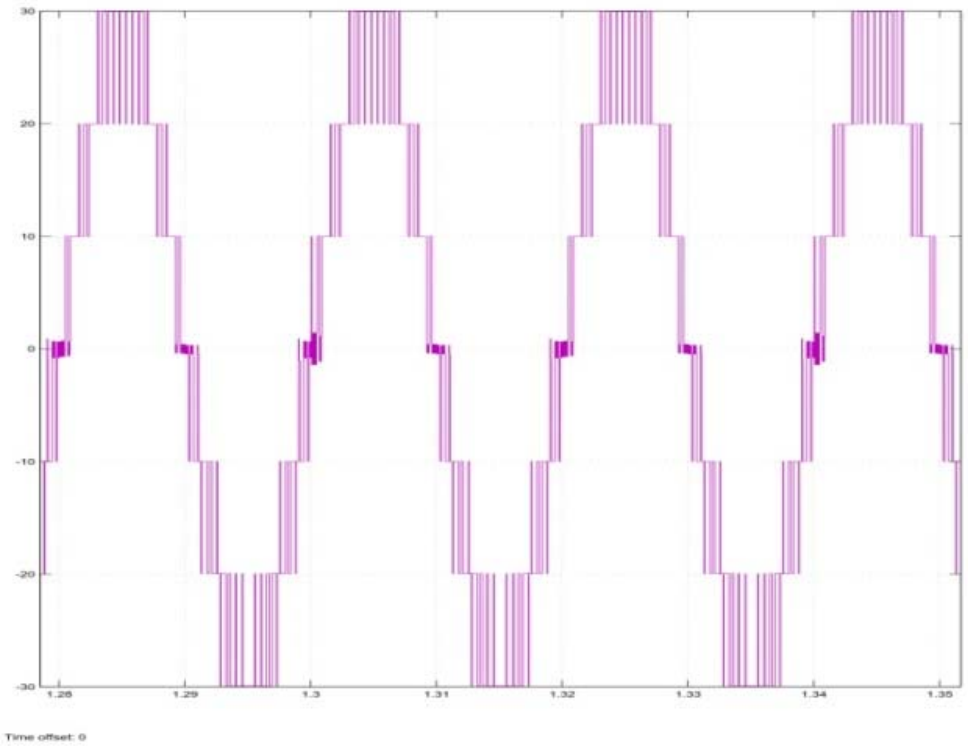

Fig9: Output voltage of seven level inverter

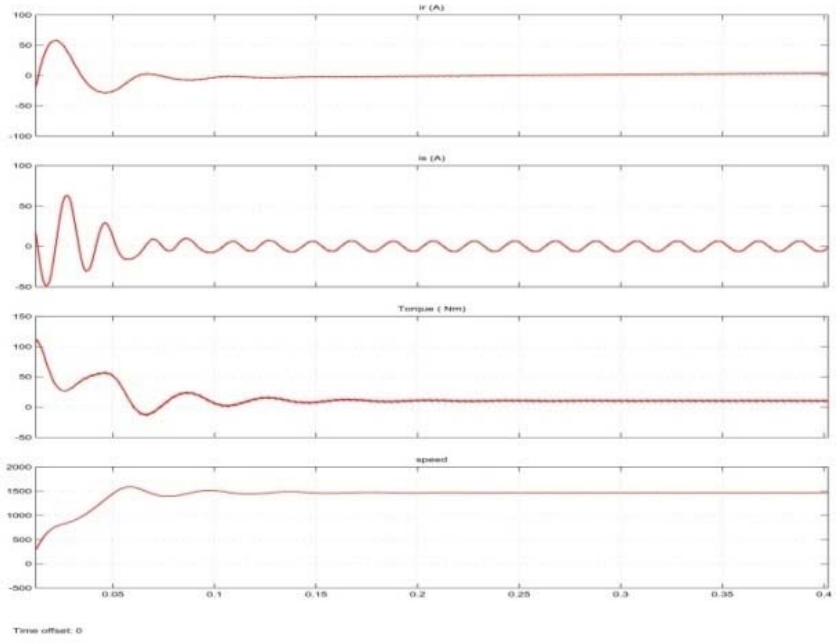

Fig10: Performance of induction motor drive

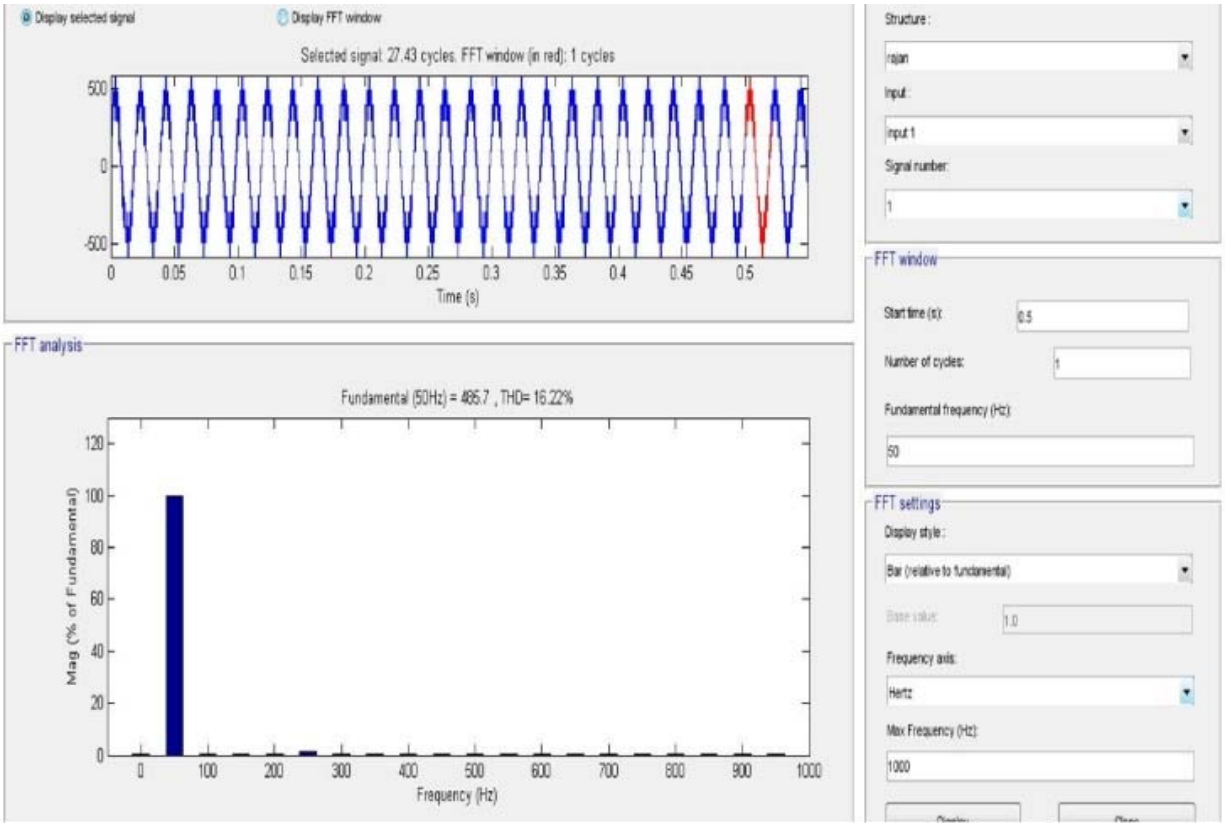

Fig11: FFT spectrum of seven level inverter voltage

Output Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
Vdc/3	0	1	0	1	1	0	1	1	0	0
2Vdc/3	0	1	1	0	0	0	1	1	0	0
Vdc	1	0	0	0	0	0	1	1	0	0
0 Vdc	0	1	0	1	0	1	1	1	0	0
-Vdc/3	0	1	0	1	1	0	0	0	1	1
-2Vdc/3	0	1	1	0	0	0	0	0	1	1
-Vdc	1	0	0	0	0	0	0	0	1	1

Table2: Switching sequence of multilevel

inverter using 10 switches

5. A 5 switches multilevel inverter topology

5.1 .Circuit Description

The proposed five switched topology has been introduced in Fig.12. The Fig.13 shows the simulation of three phase circuit of proposed topology. It is about modifying or reducing single switch from 10 switches topology obtaining the tag of 5 switches configuration. The proposed 5 switches topology is simpler design compared to all conventional topologies. This proposed topology method using generalized expression for the output voltage level is

$$V_O = (2 * S_n - 3)$$

Where V_o = Number of output voltage level

S_n= Number of switches

$$V_0 = (2 * V - 1)$$

Where V = Number of DC sources

To obtain the unique pulse pattern and trigger the switches at the proper instant, switches S_1 ,S_2 and S_3 get compulsorily unidirectional, otherwise the output waveform will get distorted. The system is more compact anduser friendly by using reduced number of switches. The seven levels MLI result in less utilization of sources through the usage of the four separate dc sources for the generation. Number of H-Bridge is used and it plays 2 switches producing reversal polarity. Table.3 represents the switching scheme for the proposed topology. The output voltage waveform & performance curve of induction motor is shown in Fig 14&15 respectively and the total harmonic output is noted in Fig.16.

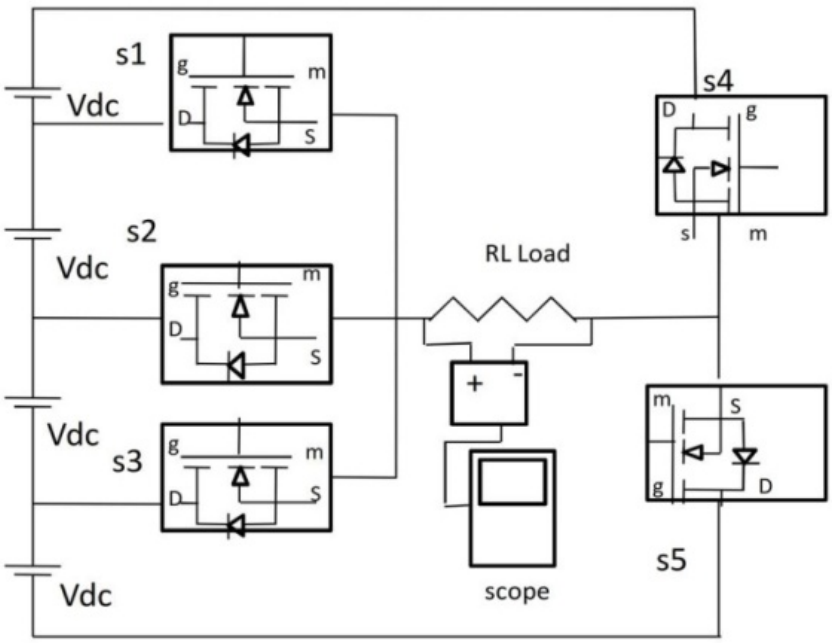

Fig12: Proposed multilevel inverter using 5 switches

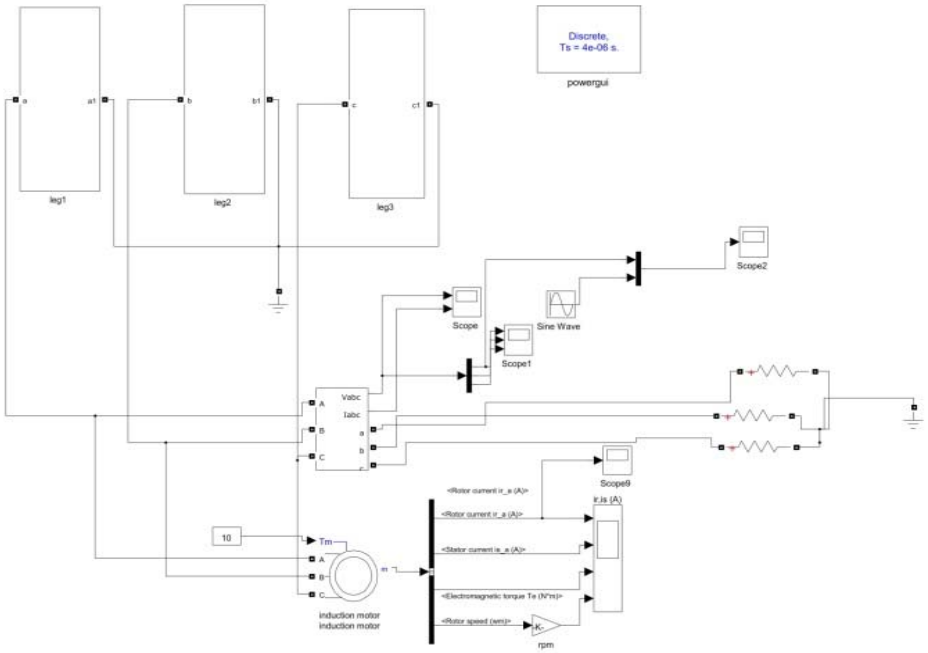

Fig13: Three phase multilevel inverter using 5 switches

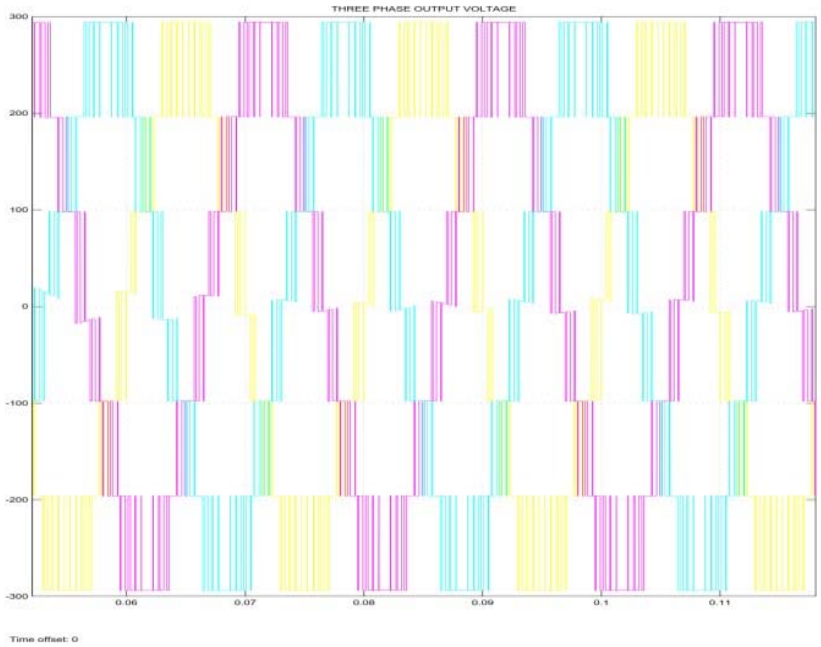

Fig14: Output voltage of seven level inverter

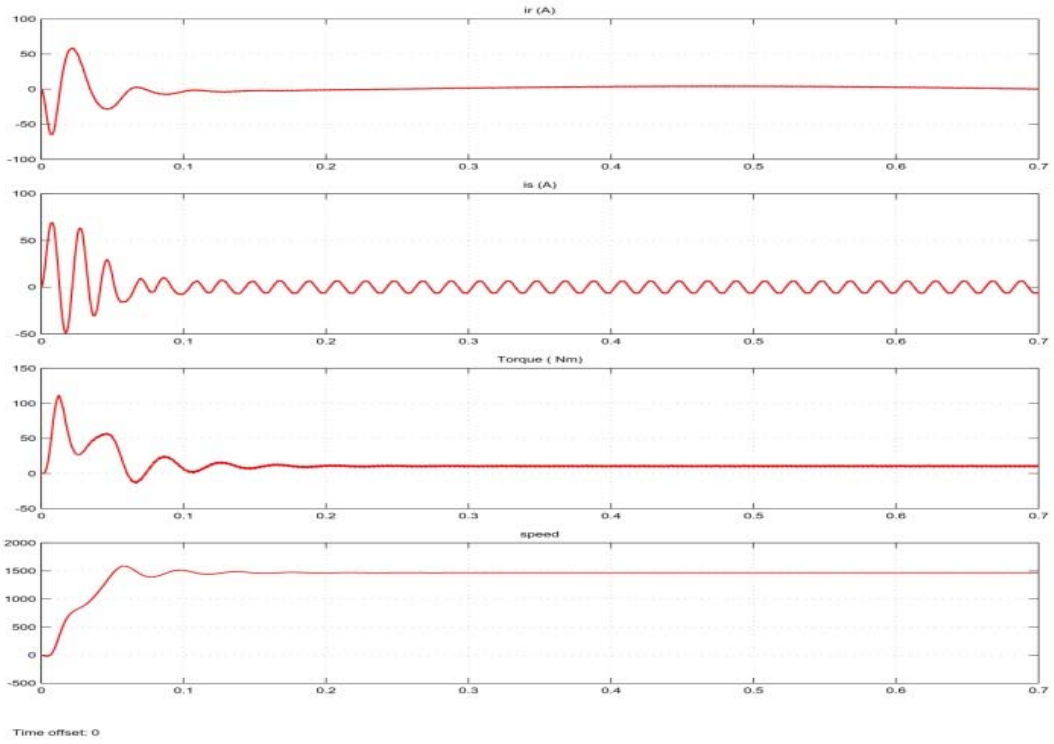

Fig15: Performance of induction motor drive

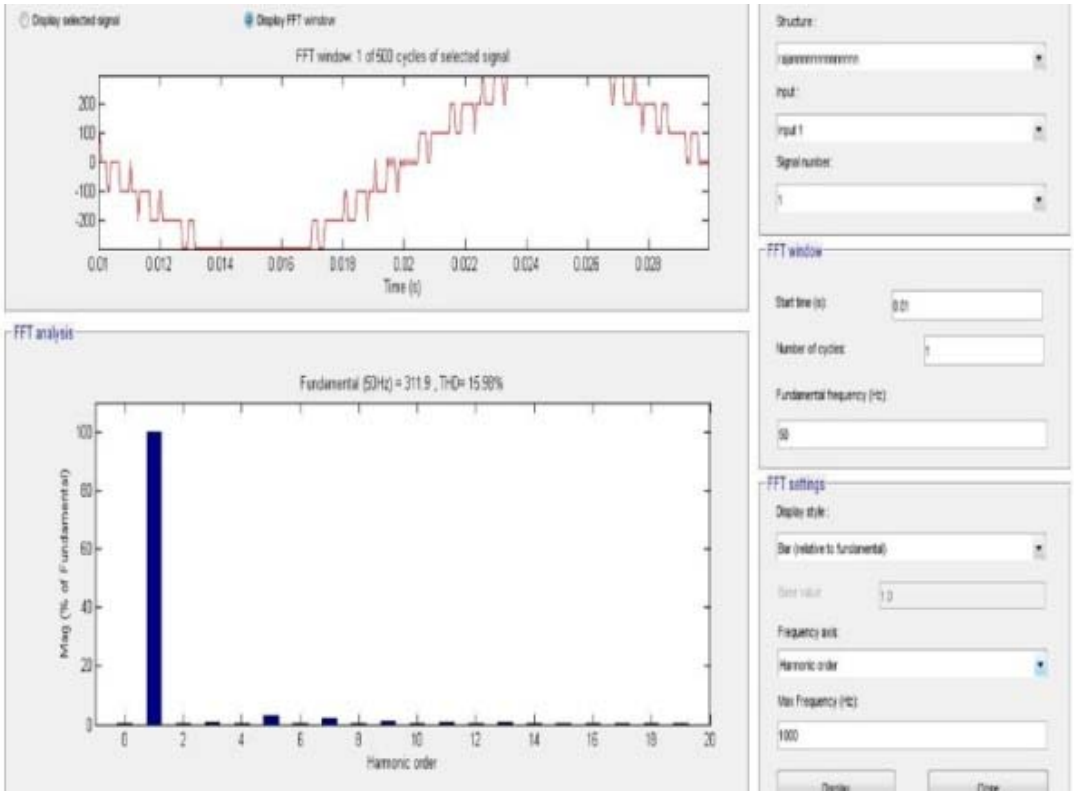

Fig16: FFT spectrum of seven level inverter voltage

Output Voltage	S_1	S_2	S_3	S_4	S_5
V_{dc}	0	0	1	0	1
$2V_{dc}$	0	1	0	0	1
$3V_{dc}$	1	0	0	0	1
$0V_{dc}$	0	0	0	0	0
$-V_{dc}$	1	0	0	1	0
$-2V_{dc}$	0	1	0	1	0
$-3V_{dc}$	0	0	1	1	0

Table3: Switching sequence of multilevel inverter using 5 switches

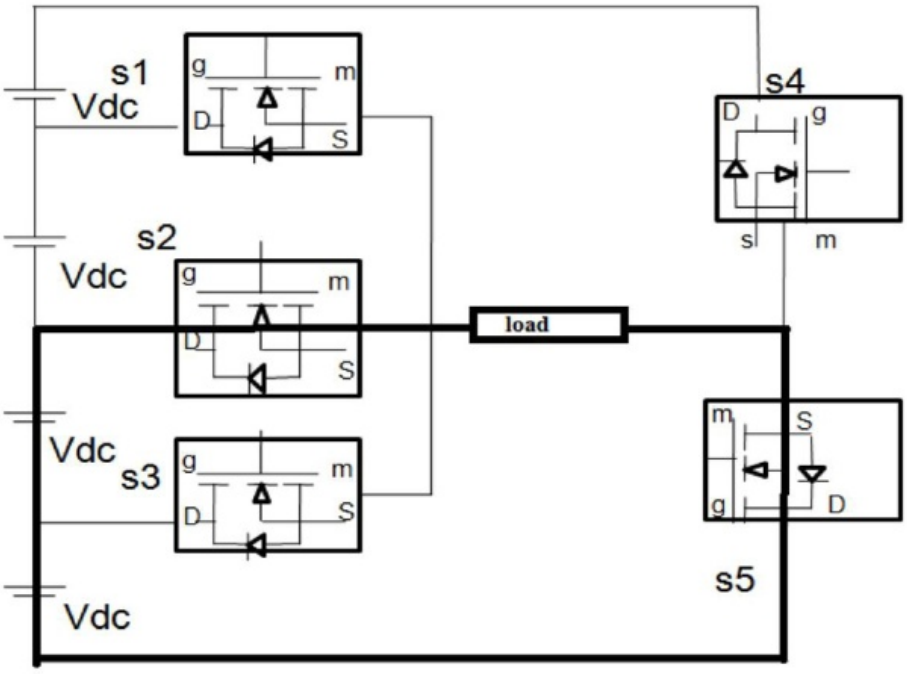

Fig17: Switching sequence required to generate output voltage level V_{dc}

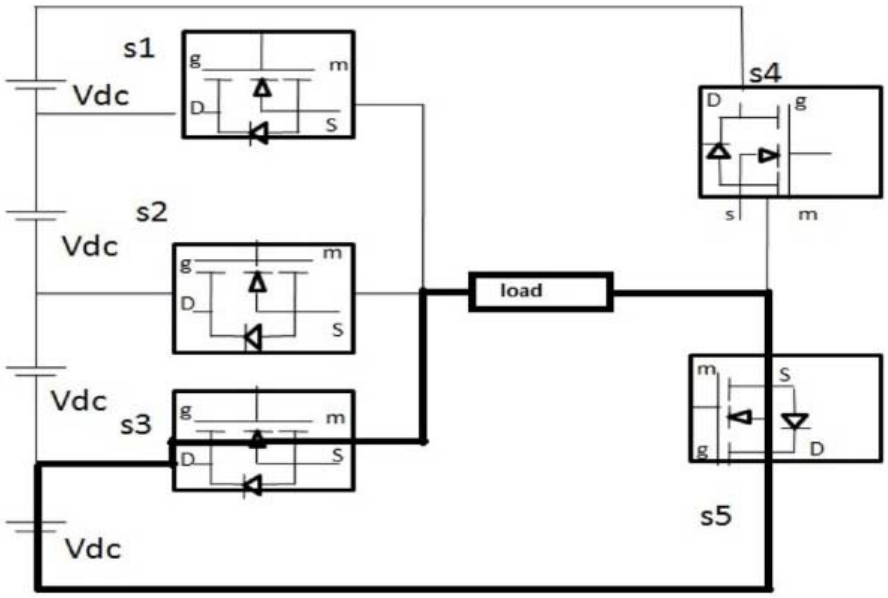

Fig18: Switching sequence required to generate output voltage level $2V_{dc}$

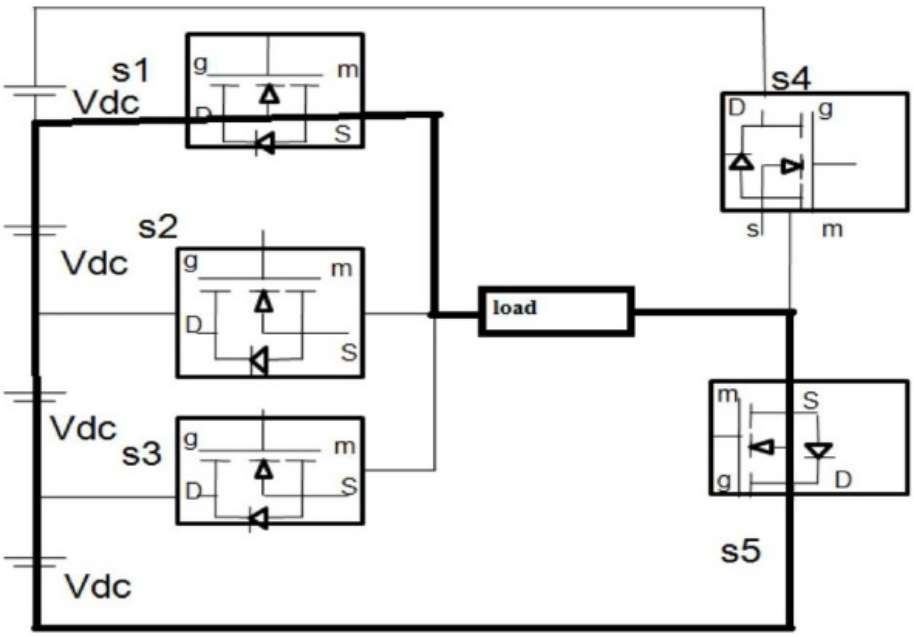

Fig19: Switching sequence required to generate output voltage level $3V_{dc}$

Multilevel inverter Type	Cascaded 12 Multilevel Inverter	10 switches multilevel inverter	5 switches multilevel inverter
Main Switches	12	10	5
Capacitor	-	3	-
Voltage Sources	3	1	4
THD (%)	19.97	16.22	15.98

Table4: Comparative evolution of multilevel inverter.

5.2. Power Stage Operation

The switching sequences for the generation of positive levels (0, V_{dc}, $2V_{dc}$, V_{dc}) named as level 0, level 1, level 2, level 3 are as shown in Table 3. According to the table, there are four possible switching states to control the inverter. The required output positive voltage levels produced by the level generator are generated as follows:

1) Zero output level: S_1, S_2, S_3, S_4, S_5 are OFF in the generation of zero voltage (0 level) is shown in Table 3.

2) V_{dc} output voltage level: S_3,S_5 are ON. All the other switches are OFF resulting in the generation of 1 v_{dc}. Fig.17 shows the current paths that are active at this stage.

3) $2V_{dc}$ output voltage level: S_2,S_5 are ON. All the other switches are OFF resulting in the generation of 2 v_{dc}. Fig.18 shows the current paths that are active at this stage.

4) $3V_{dc}$ output voltage level: S_1,S_5 are ON. All the other switches are OFF resulting in the generation of 3 V_{dc}. Fig.19 shows the current paths that are active at this stage.

5. comparative Evaluation

In order to clarify the advantages and disadvantages of the proposed topology, it should be compared with the different kinds of topologies presented in this paper. In the comparison the number of switches, DC bus capacitor, Voltage sources and THD are taken and tabulated in Table.4.

6. Conclusion

In this paper, a new topology with 10 switches and 5 switches is introduced and the same 7-level output is observed in either of the cases and shows the performance result of induction motor. Circuits are simulated using MATLAB/SIMULINK software and total harmonic distortions are obtained. It can be seen that the 5-switch topology is better than other presented topology because it requires a lesser number of switch and also THD content is lower in comparison with other mentioned topology.

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