Virtual Laboratory: Switching of A Nearly Resistive Load

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Abstract: - The Corona pandemic has also a strong impact to the way of teaching. The knowledge of the influence of parasitic inductors is very important for future Electronics and especially Power Electronics engineers. Practical laboratory experiments are therefore very helpful! During the study year 2020/21 even laboratory exercises were transferred to online sessions. A successful series of experiments which help very much to understand the function of inductors and the large influence of the wiring was also transferred to the web. The object of these experiments is to show the influence of parasitic inductances and how to keep their influence small. The experiments are explained and the advantages and disadvantages of the virtual laboratory are discussed.

Key-Words: - virtual laboratory, inductive load, parasitic inductance, wiring, switching, overvoltage

1 Introduction

The author has carried out these laboratory exercises for more than three decades. These exercises are very successful in getting a better understanding of the influence and the effect of inductors. You can tell the students a thousand times that

$$u_L = L\frac{di_L}{dt} \ , \qquad (1)$$

that a voltage across an inductor changes the current, that a change of the current produces a voltage, or you can explain the induction law etc., but when you are present with them in the laboratory you have to recognize that they have not understood it at all. The necessary material for our experiments is very simple: a power supply with about 12 V, a pulse generator with e.g. 10 kHz with an output voltage of -10 V and 10 V, a winded resistor around a ceramic kernel of e.g. 22 Ω resistor (Fig. 1), a MOSFET with a maximal drain voltage of about 450 V, 1 m long cables with banana connectors, clamps, and a coaxial cable for the connection of the pulse generator with the transistor. Later on we need a diode and a small capacitor. We change the values of the input voltage and the resistor for the different groups of students. With the rectangular signal from the pulse generator, the MOSFET is turned on and off periodically. We measure the drain-source and the gate-source voltages. Fig. 2 shows the whiteboard sketch of the circuit. An excellent book treating the basics of power electronics is [1].

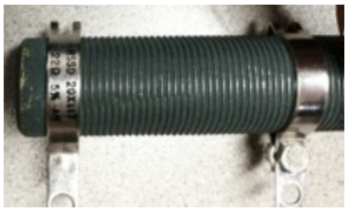

Fig. 1. Load resistor

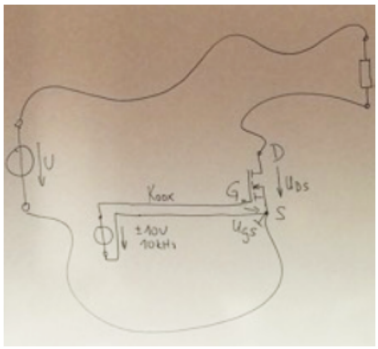

Fig. 2. Sketch of the circuit

At first we discuss the expected signal forms. After some trials the results are a rectangular signal between gate and source with plus/minus 10 V, and a voltage between the input voltage and approximately zero across drain-source. When the gate signal is high, the transistor is turned on and the voltage across it is nearly zero.

Due to the pandemic situation in the study year 2020/21 all lectures including also the laboratory work were transferred to online lectures carried out by Zoom sessions. The virtual exercise is presented in detail and the pros and contras are discussed.

2 Virtual Exercise

The cables are 1 m long and lie arbitrarily on the table. Therefore, in the simulation no straight lines are drawn. The coaxial cable for the control, however, is symbolized by straight lines. The generator has an output resistor of 50 Ω.

2.1 Experiment 1: ideal devices

This is an idealized experiment (Fig. 3) which cannot be done in reality. The results are equal with the ones which were achieved by consideration (Fig. 4). All simulation can be done with LT Spice and this program can be downloaded for free from Analog Devices.

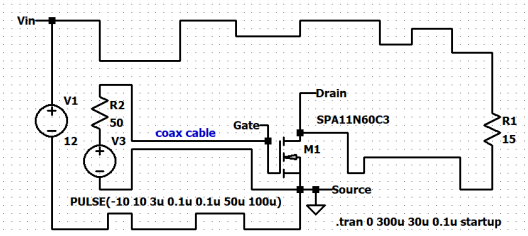

Fig. 3. Circuit diagram with idealized devices

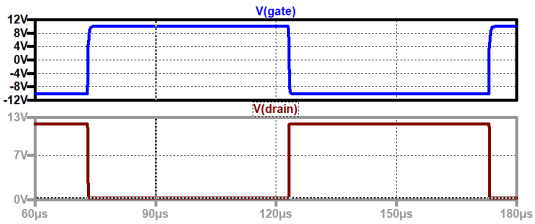

Fig. 4. Experiment 1 up to down: gate and drain voltage

2.2 Experiment 2: consideration of the parasitic inductance of the resistor

The resistor has a parasitic inductance. This will be included in the circuit (Fig. 5).

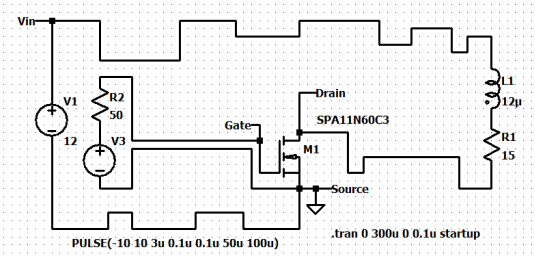

Fig. 5. Circuit diagram with parasitic inductance of the load included

The upper channel shows the control signal and the lower one depicts the drain voltage (Fig. 6). As expected the voltage across the transistor is about zero, when the gate signal is high and equal to the input voltage, when the control signal is low. But when the control signal goes down to zero, something strange happens. (In the laboratory the attenuator of the oscilloscope for channel two would yield a picture like in Fig. 6).

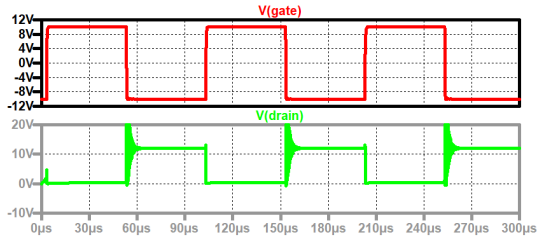

Fig. 6. Experiment 2, up to down: control signal, drain-source voltage

The voltage across the transistor reaches a higher value than 20 V. Great astonishment! Why is the voltage higher than the supply voltage? Now they students have to measure the voltage across the electronic switch exactly and figure out what has happened. Removing the limitation in channel 2 leads to Fig. 6.

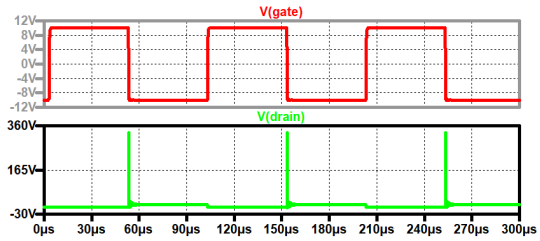

Fig. 6. Experiment 2, up to down: control signal, drain-source voltage (not limited)

Expanding the turn-off event leads to Fig. 7.

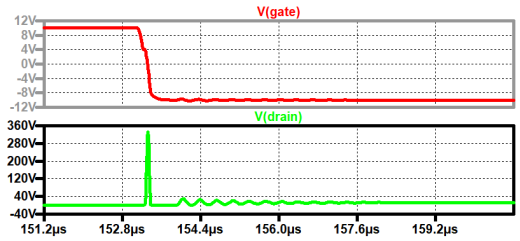

Fig. 7. Experiment 2, up to down: control signal, drain-source voltage, turn-off expanded

The voltage goes up to 330 V, nevertheless, the input voltage is only 12 V! (It takes some time until the students recognize that this is caused by the parasitic inductance of the resistor, especially in the real laboratory). In the virtual lab it is easier to check, because the load inductance can be seen in the circuit diagram.
At this point one has also the possibility to explain a little about the switching behavior of the MOSFET e.g. Miller plateau, gate current (c.f. Fig. 8).

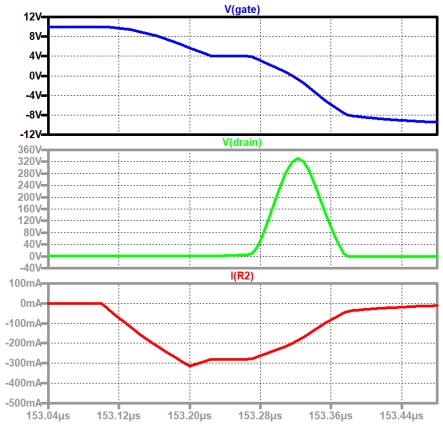

Fig. 8. Experiment 2, turn-off, up to down: voltages across gate, drain, and gate current (measured through the output resistor of the generator)

Due to the fact that the resistor has a parasitic inductance an overvoltage occurs. During turn off the current decreases fast inducing a large negative voltage across this inductor. From Kirchhoff's voltage law one knows that the sum of all voltages must be zero. When a large negative voltage is produced at the parasitic inductor, this voltage must be compensated to achieve zero voltage across the loop. Therefore, the voltage across the switch (transistor) gets so high.

2.3 Experiment 3: reducing the over-voltage

When the transistor is turned off, the current through the inductor must find a new path. This can be achieved by a free-wheeling diode. The diode is connected by cables of again 1 m length (Fig. 9).

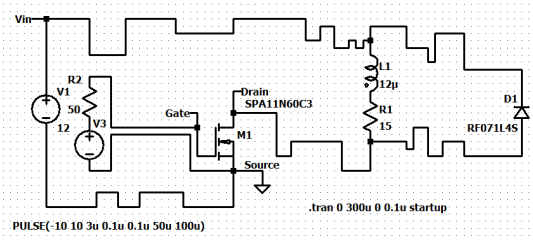

Fig. 9. Experiment 3: with free-wheeling diode

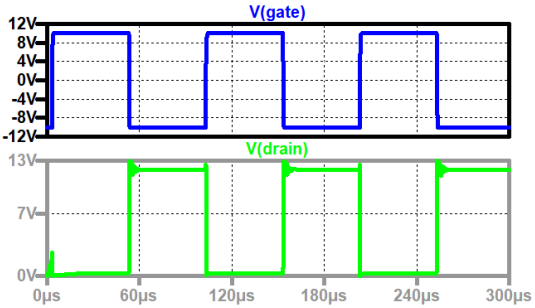

Fig. 10. Experiment 3, up to down: control signal, drain-source voltage

Fig. 10 shows again the control signal and the drain voltage. The overvoltage is now limited to the forward voltage of the diode. When the current reaches zero and the free-wheeling diode turns off, a small decreasing ringing occurs.

2.4 Experiment 4: the realistic circuit

In reality it is not so easy. Each cable can also be interpreted to have an inductive part. These parasitic inductors are now included into the circuit (Fig. 11). The results shown in Fig. 12 are similar to the ones which could be seen on the oscilloscope. The first finding in the real laboratory would be (after some wrong ideas) that the resistor has an inductive component (due to the winding of the resistor material). The drain-source voltage reaches 400 V with an input voltage of only 12 V. The discussion would lead to the idea that a path for the current through the load inductance must be generated, that a diode should be connected in parallel to the load.

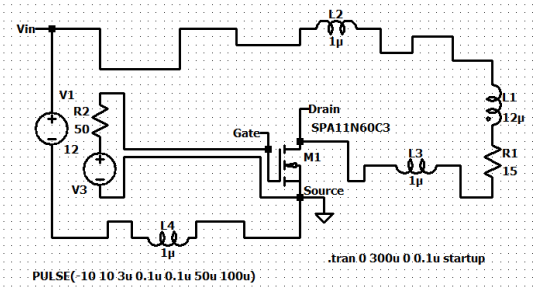

Fig. 11. Experiment 4: the realistic circuit

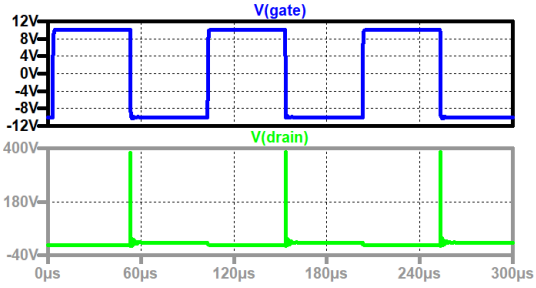

Fig. 12. Experiment 4, up to down: control signal, drain-source voltage

2.5 Experiment 5: use of a free-wheeling diode

The free-wheeling diode should be connected with cables which are one meter long. In the circuit diagram the cables are again symbolized by zig-zag lines with an inductor in between (Fig. 13). The results are shown in Fig. 14. The voltage across the transistor is reduced as expected, but is still much too high (200 V)! In the real laboratory at this point we have astonished silence and it takes some time until the students accept that it is caused by the cables! In the virtual laboratory it is easier, because

we have included the inductive effect by concrete coils. The overvoltage is induced by the wiring.

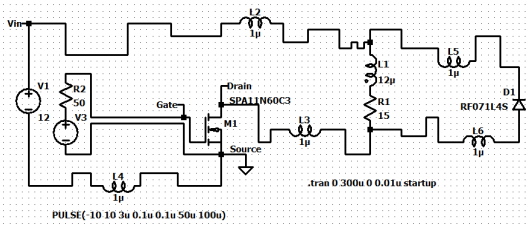

Fig. 13. Experiment 5: with free-wheeling diode

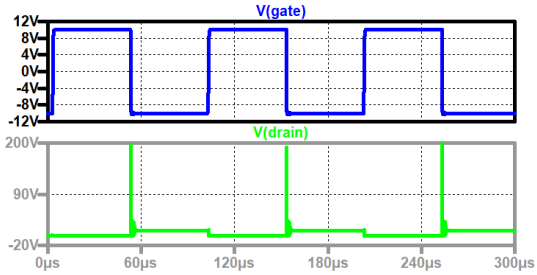

Fig. 14. Experiment 5, up to down: control signal, drain-source voltage

What does this mean in reality? One has to make all wires, in which the current changes fast, as short as possible to reduce loops which produce inductance. The loops must be as short and small as possible. This is the case in experiment 3 (ideal wiring). After this finding one can talk about the design of printed circuit boards. In a next step we discuss what to do when it is not possible to realize short wires.

2.6 Experiment 6: when long cables are necessary

Sometime in practice one has a wiring task where it is not possible to build a compact system. Take for example a motor for a window mover or other auxiliary propulsion systems in a car. The supply comes from the car battery and the electronic is mounted on a fixed place. It is clear that it is not possible to combine battery, electronics and load at one place. Load, battery and electronics are mechanically far from each other. What to do?

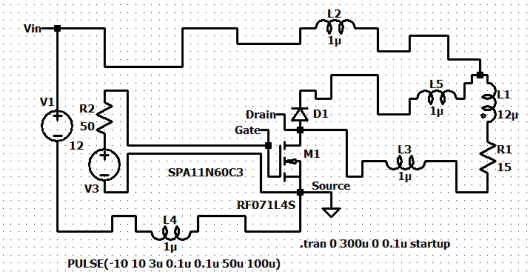

Fig. 15: Experiment 6: optimal position of the diode

Looking at the circuit in Fig. 13 one can see that five cables are used. The only device the position of which can be changed is the diode (the source, the load, and the electronic switch are at fixed places in the car). One can connect the diode directly to the drain of the switch. So one cable can be removed and only four cables are now necessary. This is shown in Fig. 15.

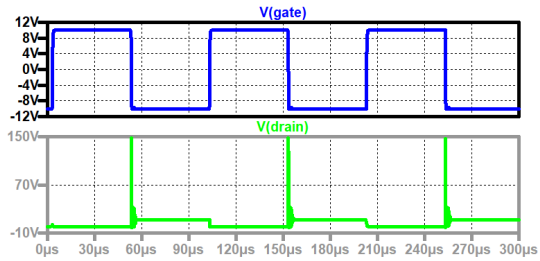

Fig. 16. Experiment 6, up to down: control signal, drain-source voltage

There is a significant reduction of the overvoltage due to the reduction of one wire. But it is still much too much overvoltage.

2.7 Experiment 7: what to do next?

When we look at the inductors L3 and L5 we recognize that L3 is in series to the load inductance, therefore its current flows either through the switch or through the diode. This inductor has a free-wheeling path as has the load inductor and is therefore harmless. But when one looks at L5, it is different. When the transistor is turned on no current flows through L5, but when the transistor turns off, the diode turns on and current flows through it with large positive derivative. This current rise produces a high positive voltage.

At this point it is time for a discussion what to do. What can we do to avoid the voltage spike? This process lasts often more than a quarter of an hour. We know from physics that no voltage is induced only when the current does not change. The only counter-measure is that the current in L5 does not change. The same current must flow independently whether the switch or the diode are conducting. Now sometimes adventurous concepts are proposed. The solution is a small change in the wiring like in Fig. 17. Now always the same current flows through L5 independent whether the switch or the diode is conducting and the overvoltage is reduced. Now it is also all one how long the cables are and how large the inductance of the load is! The overvoltage is now only produced by the cables from the supply voltage (Fig. 18). This small change in the wiring has an important impact on the design.

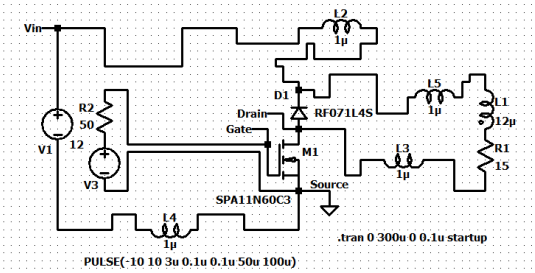

Fig. 17. Experiment 7: change in the wiring

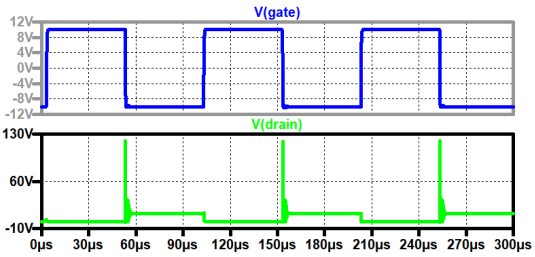

Fig. 18. Experiment 7, up to down: control signal, drain-source voltage

2.8 Experiment 8: reduction of the influence of the supply lines

Now we have to eliminate the influence of the supply lines. When the transistor turns off, the current in the supply lines must find an easy new path. Now a discussion is necessary. The result is to connect an avalanche diode or a capacitor in parallel to the branch cathode and source. The capacitor is the cheaper variant and will be implemented (Fig. 19).

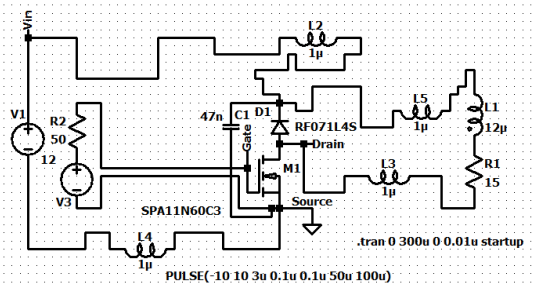

Fig. 19. Experiment 8: reduction of the influence of the supply lines

The capacitor has to be connected in the shortest possible way to avoid additional inductance. The capacitor is functionally parallel to the source and in steady-state it is charged equal to the input voltage. When the transistor is turned off, the current in the input line charges the capacitor and its voltage increases. When the current reaches zero, the voltage across the capacitor reaches its maximum and now the current changes its direction and begins to discharge the capacitor. The capacitor will be discharged to a value lower than the input voltage and the current changes its direction and charges again the capacitor. The inductance of the wires and the capacitor form a resonant circuit and a ringing occurs. The ringing is damped by the losses in the wires and by the series resistor of the capacitor (Fig. 20).

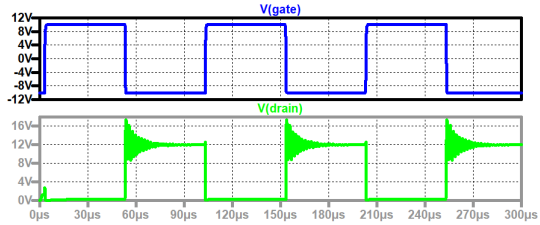

Fig. 20. Experiment 7, up to down: control signal, drain-source voltage

Fig. 21 shows the enhanced turn-off. The ringing depends on the capacitor and on the sum of the inductors L2 and L4. In the uppermost picture the current through the load is shown. One can see that the current decreases according to the time constant of the load very fast (the inductance value is the sum of the inductances of the load and the of the connection wires). The main result of our investigations is that in reality even small parasitic elements have a large impact on the function of a circuit.

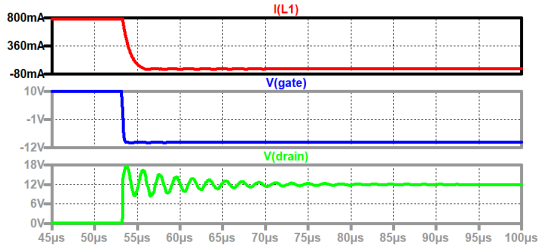

Fig. 21. Experiment 7, turn-off up to down: load current, control signal, drain-source voltage

To further reduce the overvoltage a larger capacitor can be used, using e.g. a tantalum capacitor with a value of 3,3 µF the ringing can be suppressed (Fig. 22).

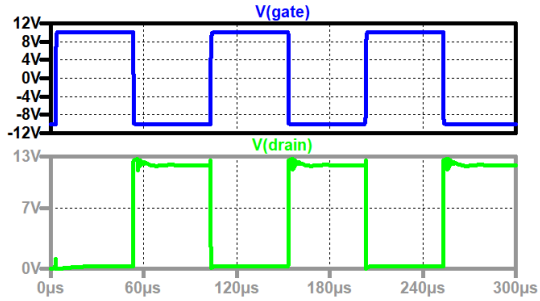

Fig. 22. Experiment 7 with larger capacitor, up to down: control signal, drain-source voltage

3 Further Evaluation

3.1 Interpretation of Experiment 4

The circuit of experiment 4 can be interpreted as an ideal switch S, a resistor R which consists of all resistive elements in the loop (load, wires, on-resistor of the transistor), and an inductor L, in which all inductances (wires, load) are summed up (Fig. 23).

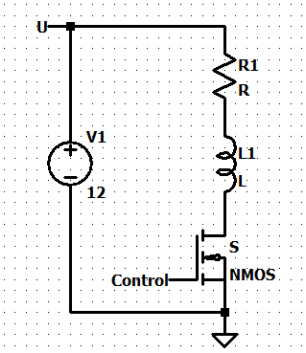

Fig. 23. Concentrated circuit diagram for experiment 4

Therefore, one can write (small letters represent time functions) after the turn-on of S

$$U = R \cdot i + L\frac{di}{dt} \quad . \tag{2}$$

Laplace transformation leads to

$$\frac{U}{s} = R \cdot I(s) + L \cdot s \cdot I(s) \, . \tag{3}$$

The current increases after the turn-on by an e-function

$$i = \frac{U}{R}\exp(-\frac{1}{RC}t) \, . \tag{4}$$

When the transistor is turned off, the current flows through the parasitic capacitor of the transistor. The loop can be described according to

$$U = R \cdot i + L\frac{di}{dt} + \frac{1}{C}\int_0^t i \cdot dt \, . \tag{5}$$

The starting point is the turn-off moment of the transistor, the channel of the MOSFET vanishes and the current has to commutate into the parallel capacitor. The current through the inductor is at this moment U/R. The Laplace transformation leads to

$$\frac{U}{s} = R \cdot I(s) + L \cdot \left(s \cdot I(s) - \frac{U}{R} \right) + \frac{1}{C}\frac{1}{s} \cdot I(s) \tag{6}$$

and results in

$$I(s) = U \frac{\frac{1}{L} + \frac{s}{R}}{\left(s + \frac{R}{2L} \right)^2 + \left(\frac{1}{LC} - \frac{R^2}{4L^2} \right)} \, . \tag{7}$$

From the function in the frequency domain one can learn that a damped ringing occurs with the damping factor

$$\delta = \frac{R}{2L} \tag{8}$$

or the time constant

$$\tau = \frac{2L}{R} \, . \tag{9}$$

and an angular frequency of

$$\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \, . \tag{10}$$

When the voltage across the capacitor (that is equal to the voltage across the transistor) has a maximum, the current reaches zero. Looking at the measurement, or in our case on the simulation, shows that the voltage starts now to decrease and goes down to zero. That shows us that the current must now be negative. One would expect that when the voltage reaches a minimum it would increase again. But that does not happen, the voltage is zero and after a longer time period rings up again. Therefore, we can conclude that the model is not valid anymore! The reason is the body diode of the of the MOSFET. The circuit can be described again by (2) with the initial condition of the maximum negative value of the current. Now the current increases again by an e-function; when the current reaches zero, an ideal diode would turn-off, but in reality the body diode turns off at an already positive value, due to the reverse recovery effect. Now a ringing starts and the described process repeats again. Fig. 24 shows the equivalent circuits. During the transient caused by the turn-off of the transistors, the models b and c alternate. The next turn-on starts with model Fig. 24.a again.

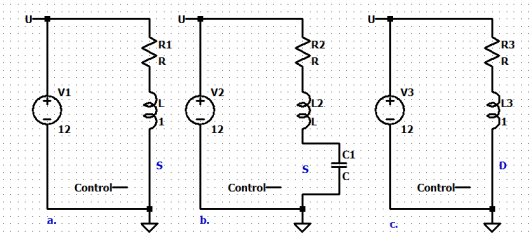

Fig. 24. Equivalent circuits

3.2 Estimation of the overvoltage

In this subsection the overvoltage across the electronic switch shall be estimated. We simplify the equivalent circuit according Fig. 24.b by omitting the resistor, but one must include the current U/R as initial condition. The initial condition for the capacitor is zero, because the transistor was turned on and the capacitor therefore shunted. The circuit can be described by the state equations

$$\frac{di_L}{dt}=\frac{U-u_C}{L} \qquad i_L(0)=\frac{U}{R} \tag{11}$$

$$\frac{du_C}{dt}=\frac{i_L}{C} \qquad u_C(0)=0\ . \tag{12}$$

The Laplace transformation leads therefore to

$$\begin{bmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & s \end{bmatrix}\begin{pmatrix} I_L(s) \\ U_C(s) \end{pmatrix}=\begin{pmatrix} \frac{U}{L\cdot s}+\frac{U}{R} \\ 0 \end{pmatrix} \tag{13}$$

Using Cramer's rule, the voltage across the capacitor (that is also the one across the transistor) can be written as

$$U_C(s)=\frac{\frac{U}{LC\cdot s}+\frac{U}{RC}}{s^2+\frac{1}{LC}}=U\left(\frac{\frac{1}{LC}}{s\left(s^2+\frac{1}{LC}\right)}+\frac{\sqrt{LC}\,\frac{1}{RC}\sqrt{\frac{1}{LC}}}{s\left(s^2+\frac{1}{LC}\right)}\right) \tag{14}$$

and in the time domain according to

$$u_C(t)=U\left(1-\cos\sqrt{\frac{1}{LC}}t+\frac{1}{R}\sqrt{\frac{L}{C}}\sin\sqrt{\frac{1}{LC}}t\right). \tag{15}$$

The output capacity of the transistor is small, therefore, one can estimate the overvoltage by

$$\hat{U}\approx U\frac{1}{R}\sqrt{\frac{L}{C}}\ . \tag{16}$$

3.3 Design of the capacitor to reduce the overvoltage caused by the supply lines

We have seen in the experiment 8 that a capacitor is necessary in parallel to the branch cathode of the diode and source of the MOSFET. When the transistor is turned off, the current through the input wires (summarizing their inductors L2+L4 leads to L_S) can commutate into the capacitor C_S (we call the capacitor C_S to distinguish it from the output capacitor of the switch, which was called only C for simplicity). The capacitor is charged equal to the input voltage. When the transistor S turns off, we get the loop

$$U=L_S\frac{di}{dt}+\frac{1}{C_S}\int_0^t i\cdot dt+U\ . \tag{17}$$

The current in the input lines is U/R at the moment when the transistor turns off. Laplace transformation leads to

$$I(s)=\frac{U}{R}\frac{s}{s^2+\frac{1}{L_SC_S}}\ . \tag{18}$$

After the back transformation one can write for the voltage across C_S

$$u_{CS}=\frac{1}{C}\int_0^t\frac{U}{R}\cos\sqrt{\frac{1}{L_SC_S}}t\cdot dt+U\ . \tag{19}$$

resulting in

$$u_{CS}=\frac{U}{R}\sqrt{\frac{L_S}{C_S}}\sin\sqrt{\frac{1}{L_SC_S}}t+U\ . \tag{20}$$

The maximal reached overvoltage is therefore

$$U_{CS,\max}=\frac{U}{R}\sqrt{\frac{L_S}{C_S}}\ . \tag{21}$$

The capacitor to achieve an overvoltage of maximal $U_{CS,max}$ can now be calculated according to

$$C_S=\left(\frac{U}{R\cdot U_{CS,\max}}\right)^2L_S\ . \tag{22}$$

4 Conclusion

The here described series of experiments was carried out over many years successfully. They helped the students in the Bachelor course of Electronics to get some understanding of the effect of inductors and especially of the influence of parasitic ones on the circuit design. The extreme simplicity (only a few devices are necessary) and the step by step way helped very much to get a better knowledge of the impact of inductors. It is important that there is enough time for thinking and rethinking and that the students are guided to find the correct results. This means that the lecturer must be busy and concentrated. Together with experiments with a Buck converter they helped students to choose the Master course in Power Electronics. Naturally a practical work and measurement with an oscilloscope are more impressive, but the virtual laboratory was the next to reality in the pandemic situation. The experiments 1 till 3 can only be done in the virtual laboratory, in the real world one can discuss them and draw the results (in the virtual world one can prove the results immediately). But from experiment 4 on the virtual laboratory makes the same steps as in reality. By using the virtual laboratory, it is easy to show currents (the high frequency current probes are not used in our Bachelor courses) and it is also easy to measure the voltage across floating devices (in reality a differential probe is necessary). The virtual laboratory enables also the students to repeat the experiments and to change parameters or loads. Summarizing one can say that during the pandemic situation the object of the laboratory work was fulfilled and stimulus for further treatments was given.

References:

[1] Ned Mohan, Torr M. Undeland, William P. Robbins, *Power Electronics*, John Wiley & Sons, 2003.