Platform for the Research of Energy Quality in Cascaded Multilevel Power Converters

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Abstract— This paper presents the implementation of a platform capable of modifying electrical connections in order to obtain all configuration possibilities of the cascaded multilevel power converter with four H bridges in common source and single source sub-topologies in symmetrical and asymmetrical configurations, with a range of 3 to 81 voltage levels. The modifications in the number of stages, modulation and topology are performed via a visual interface in MATLAB®. The modulations are optimized through a genetic algorithm and the system control is carried out using a FPGA Virtex 5. The versatility of the platform allows one to obtain, from the hardware, the configuration of the converter and the modulation characteristics selected in the visual interface in a matter of seconds.

Key-Words: - Power converter, multilevel converter, PWM, FPGA, Optimization, Genetic algorithm.

1. Introduction

In terms of power inverters, the study of energy quality is a current and relevant topic of discussion [1], [2], [3] in which multi-level converters represent part the solution, due to the fact that their output voltage presents a harmonic content inferior to that of a conventional converter [4]. The other part of the solution is the corresponding supplement of the control selection [5], [6], the topology [7], the method of frequency variation [8] and the technique of modulation generation [9]. From this perspective, the converter is the element responsible for supplying electrical energy quality, provided it is of the appropriate design.

Among multilevel converters, there has been a rise in H bridge cascaded converters, due their considerable advantages compared with classic topologies such as the locking of diodes or by condensers [4], [10]. Nevertheless, among the cascaded multilevel H bridge converters, there are common source and single source sub-topologies [11]. The first only requires one source of voltage for the whole converter and the galvanic isolation between stages is achieved with the use of transformers [12]. The second sub-topology needs a source of voltage from the H-bridge and the sources should be isolated galvanically [13]. Both sub-topologies have their advantages and disadvantages. As such, this work completes the invention of a platform that facilitates the in-depth study of each sub-topology's behavior, allowing in a matter of seconds the configuration of the converter and the modulation characteristics via a virtual interface. The versatility of the platform allows the study of multiple possibilities, with the objective of comparing possible solutions in terms of energy quality and efficiency.

2. State of the Art

The appearance of the multilevel power converter was the product of Baker and Lawrence's work in 1975 [14], now known as the cascaded H bridge converter. In 1981, the first multilevel converter with three levels by means of diode fixation was presented [15]. From this patent and the respective work, there has been a wide variety of investigations in search of optimizing and improving the multilevel system of conversion [13]. The utilization of the patent's original idea is now known as a sub-topology, [14], known as single source [16]. Another proposal used the DC voltage source to power all H bridges and used transformers at the output of every bridge in order to create galvanic isolation. The

construction of the step wave was achieved through the cascaded connection of the output of the transformers. This sub-topology received the name 'common source cascade H-bridge multilevel converter'. [17], [18], [19].

In terms of the optimization of the harmonic content of the multilevel converters' modulations, numerous techniques have been proposed depending on the sub-topology used, according to the specific objective and the nature of the search for the optimal point. [20], [21], [22]. However, there are promising strategies in the line of evolutionary algorithms such as crowding of particles (PSO) [23] and genetic algorithms (GA) [24], [25], among others. Genetic algorithms are a method of classic and functional optimization, that are used as a comparison to other methods of optimization, in the same way that the mathematic expression that describes THD in terms of switching angles provides a clear criteria of evaluation of the function of optimization [9].

3. Cascaded multi-level converters

Fig. 1 shows the general diagram of a cascaded multilevel inverter with H bridges (CMLI), where the basic function can be observed, in which the form of the output waveform is constructed through the addition of the outputs of each H-bridge. [14]. The CMLI topology can be divided into two categories, depending on the relationship of the voltages at of each bridge. These categories are symmetrical and asymmetrical. They are symmetrical if the voltages in all bridges are equal and asymmetrical if the voltages are different (the relationships 1:2 o 1:3 are common).

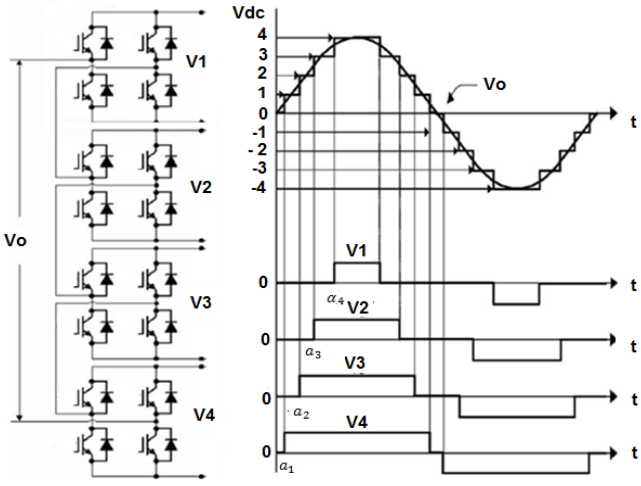

Fig 1. H-bridge multilevel converter, waveforms and converter output..

In terms of the ways of obtaining the voltage of each bridge, two sub-topologies can be described: separate DC source sub-topologies, in which all bridges are powered from separate sources (ver Fig. 2.a) and common source sub-topologies, in which all bridges are powered from the same source. The difference in voltages and the galvanic isolation is achieved through the use of transformers. (ver Fig. 2.b.). Fig. 2.c shows an example of these sub-topologies in asymmetric form with relation to 1:2. The two obtain the same output voltage wave [14].

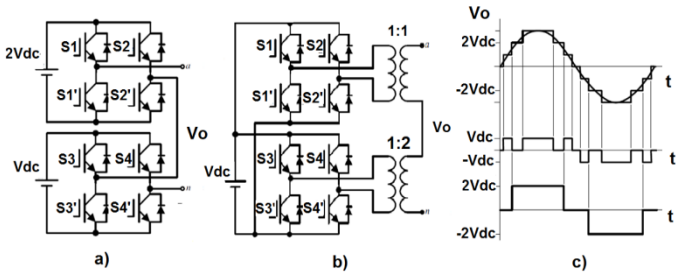

Fig. 2: Asymmetrical sub-topologies of the cascaded H bridge multilevel converter. a) Separate DC source, b) Common source, c) Output voltage.

4. Software

The software of the platform for the evaluation of converters has been implemented in a Graphical User Interface (GUI) in Matlab® and essentially relies on five processes illustrated in the main menu of Figure 3. Among these processes, is the optimization stage that allows one to locate a modulation with low harmonic content through a genetic algorithm; the second process allows the system to create modulations through the specification of switching angles of the first quarter of the wave entered directly by the user; the third process loads the data with the possibility of recovering a modulation carried out previously in the software; the fourth part of the software is the simulation of the cascaded converter that allows one to observe in detail the relevant electrical parameters and their behavior; the fifth stage implements the modulation carried out in the software with the hardware, including the specified connection characteristics. The different stages of the platform are described below:

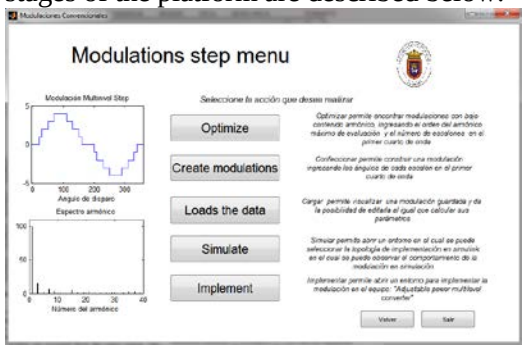

Fig. 3. GUI Main Menu.

Functionality of the optimizing process: The general process of the optimization of the software is presented in Figure 4. In order to obtain an optimized modulation, it is necessary to enter the parameters of the algorithm's functionality, which are: the number of levels of voltage of the first quarter of the wave, the order of the maximum harmonic of evaluation of THD and the maximum number of generations from the genetic algorithm. With the parameters, the search begins for the modulation with the least THDv evaluated up to the selected harmonic, and finally the genetic algorithm finds the optimum and delivers the switching angles, the form of the wave, the THD and the harmonic spectrum, among other data.

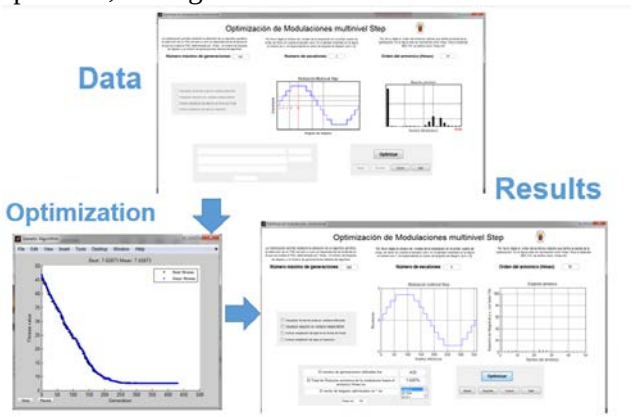

Fig. 4. Optimization process in the system.

The functionality of the optimization algorithm is shown in the flow diagram in Figure 5, in which the vector L represents the number of shooting angles by stage in the first quarter of the wave.

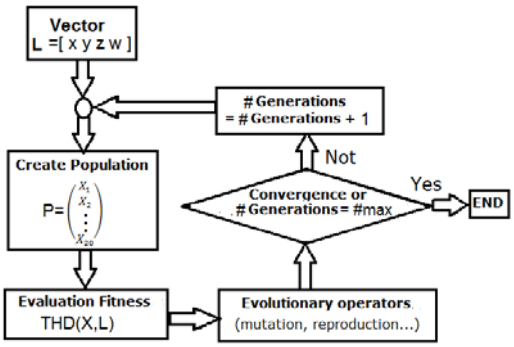

Fig. 5. Flow diagram of the optimization algorithm.

For a Step modulation, the switching angle corresponds to 1 for each level of voltage and each part of the vector indicates a voltage level [1 1 1 1 .]. The algorithm begins with a random sample and continues mutating until it arrives at a convergence, evaluating the generations using function fitness.

The process of the genetic algorithm is carried out in Matlab® through the cell GA (Genetic Algorithm) which evaluates each generation with the mathematic expression of THD, expressed in terms of the number of levels and the number of switching angles per level, which corresponds to the fitness function (Equation 1), explained in detail in [7]. The α_{ij} corresponds to the angle, j is the number of the angle, i is the number of the step, and L_i is the component i of the vector L.

$$THD = \frac{\sqrt{\sum_{n=2}^{50}\left[\frac{1}{n}\left(\sum_{i=1}^{4}\sum_{j}^{L_i}(-1)^{j-1}\cos\alpha_{ij}\right)\right]}}{\left(\sum_{i=1}^{4}\sum_{j}^{L_i}(-1)^{j-1}\cos\alpha_{ij}\right)}\cdot 100 \quad (1)$$

4.1. Process of the development of a modulation

The stage of development permits the system to produce any modulation in the range of 3-81 stages, in which the software requests the input of the switching angles of the first quarter of the wave. Each angle corresponds to the change in a level of voltage. The THD and the harmonic spectrum are updated with the change of any switching angle evaluated to the maximum harmonic selected. This process is shown in Figure 6. Upon completing the development, one can store the modulation for later analysis, simulation and implementation.

Fig. 6. Modulation development using the Graphical User Interface.

Process of loading modulations

As the platform's interface allows the user to store modulations, a process that allows the user to read the stored modulations is of course necessary. In this process, the waveform of the modulation loaded along with the harmonic spectrum, the THD and the switching angles as observed in Figure 7 can be viewed. Yet despite its simplicity, this process provides the platform with the necessary memory capacity to use the optimized and developed modulations in the system.

Process of simulation

The general process of simulation requires the input of the specific parameters of the hardware such as voltage (common or single source), relationship of the sources (symmetrical, asymmetrical 1:2, 1:3), supply voltage and RMS value of the output. These

parameters determine the number of necessary bridges and the characteristics of the converter.

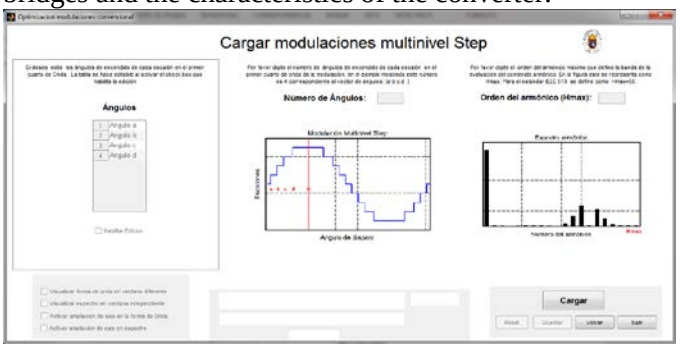

Fig. 7. Modulation loading interface.

The simulation is carried out in its totality in Simulink as demonstrated in Figure 8. The product obtained is the relevant electrical parameters of the converter.

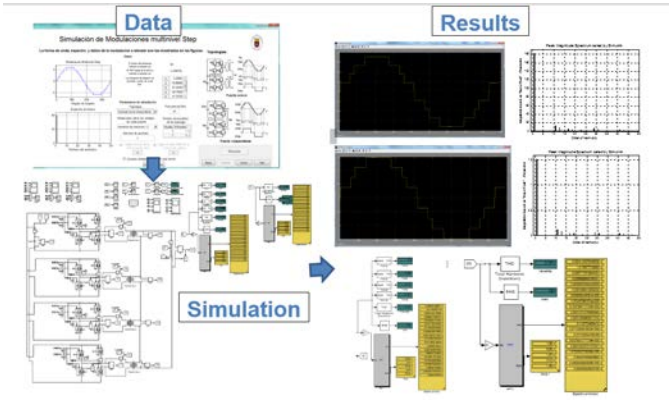

Fig. 8. Simulation .Process.

The simulation carried out is only for the power stage and has the capacity to modify the number of H-bridges, the magnitudes of the sources of voltage and the topology. The simulation includes the measurements of input voltage, input current, output voltage of each H-bridge, output voltage of the converter, output current, display of the control signals, harmonic spectrum of voltage and current, and THD of voltage and current.

Process of implementation

The implementation is the culminating process of the visual interface, in which the parameters of the converter's hardware are required, among those the topology (common or single source) and the relationship of the sources (symmetrical, asymmetrical 1:2, 1:3). The software calculates the number of H bridges necessary and the values of voltage in order to implement the modulation obtained previously. The process is divided into two stages, the first being the calculation of the electrical parameters as in the case of the drive signals of every transistor of the H bridges. The second stage is the coding of the values to be transmitted to the FPGA that is responsible for sending the switching signals to the scalable converter (hardware). The form of the interface is shown in Figure 9.

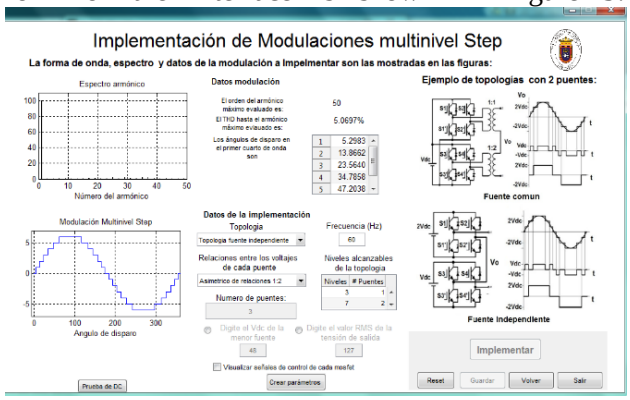

Fig. 9. Implementation using Graphic User interface.

5. Hardware

General circuit: The aim of the system is to achieve the desired flexibility with the lowest number of switches, the result being the electronic diagram shown in Figure 10. The system relies on four H bridges that permit one to obtain modulations of 3 to 81 levels of voltage, in symmetrical or asymmetrical configurations, with the highest level (81) reached with sources of asymmetrical relation 1:3:9:27, in common or single source.

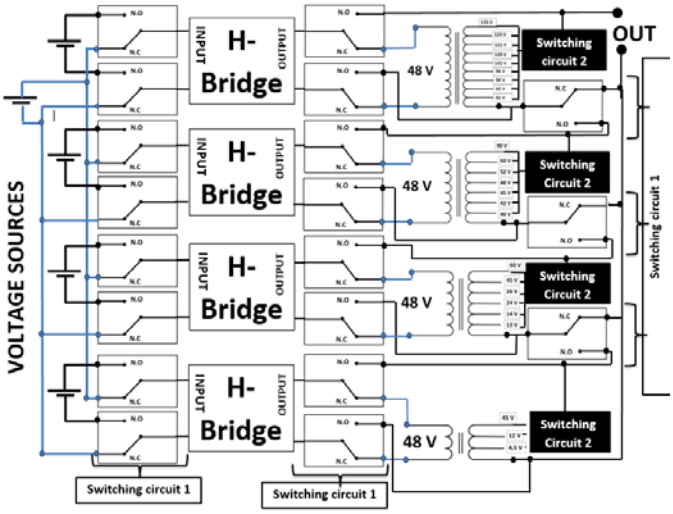

Fig. 10. Electrical diagram of the modular converter.

Stages of communication:

In order to commute the connections of the circuit's bridges, there are essentially two switching circuits. The first is responsible for making power connections and is made up of the switches shown in the electronic diagram of Figure 10. Its function is to connect the input and output of the H-bridge. At the input, it is necessary to select the type of supply of the H bridges, whether that be an isolated voltage source per bridge or that all H bridges are connected to a single voltage source. At the output, it is necessary to select the connection or de-connection

of the transformers in conjunction with the number of bridges. Additionally at the output, it is necessary to connect in cascade the outputs of the H bridges or the transformers' secondary windings. The second circuit is responsible for selecting the derivation of the transformer that is necessary to obtain the voltage values of the asymmetry selected and maintain the waveform and the RMS level of the output voltage. This works only in common source configuration. There is an extra circuit that functions simultaneously with the first and is responsible for connecting the control of the H bridges in an equal configuration to the level of power of the implemented circuits shown in Figure 11.

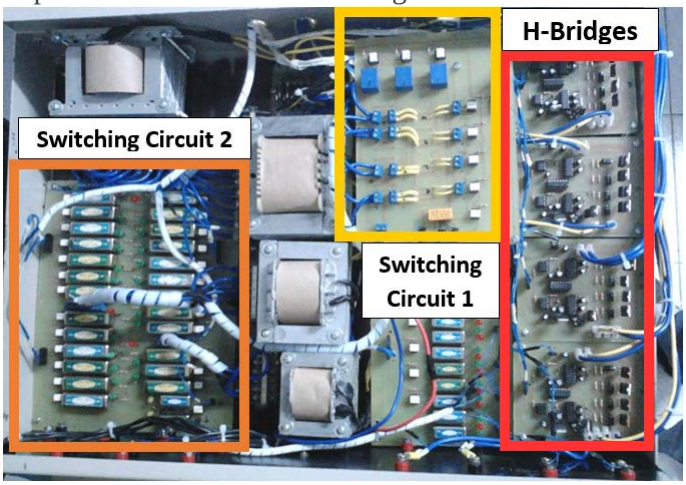

Fig. 11. Prototype of the configurable converter with 5 to 81 stages .

Platform: The hardware of the scalable converter is shown in Figure 12. This prototype consists of four H-bridges, four transformers and 32 relays that allow the configuration of deferential sub-topologies. The control was developed through an algorithm in Matlab® and the use of a FPGA XUPV5-LX110T, allowing for the adjustment of the converter in order to obtain a common or single source inverter. With 1 to 4 stages reaching modulations between 3 and 81 levels with Step modulations and PWM, the transformers are designed with a special methodology.

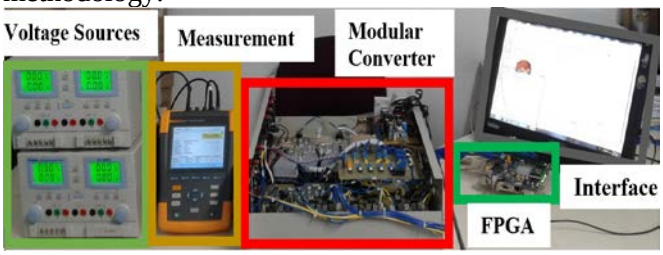

Fig. 12. Platform of the configurable converter.

6. Communication

The general diagram of communication for implementation is shown in Figure 13. The characteristics of connection and drive control are coded in order to be sent to the visual interface in an organized way, and then to be sent to the FPGA via the RS-232 protocol. The FPGA decodes the information and sends it to the conditioning circuits which provide the precise values in terms of magnitude and time in order to commute the relays and transistors.

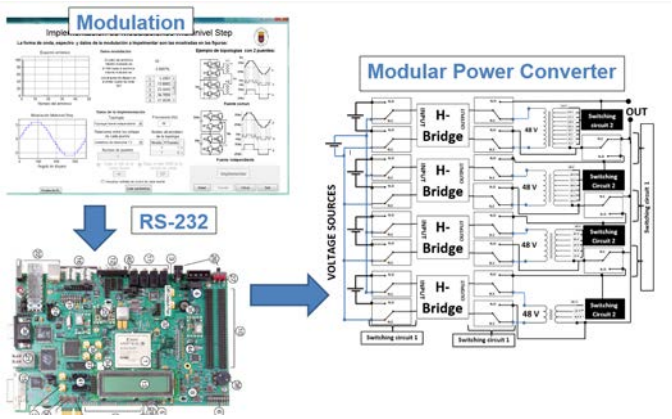

Fig. 13. General diagram of the process of implementation.

The FPGA was programmed in VHDL in such a way that it codifies the information and sends the switching signals to the conditioning circuits. For the reception of the data, the UART (Universal Asynchronous Receiver-Transmitter) is used to receive values with an input bit, 8 databits and a stop bit. In the process, FIFO buffers are used to verify the data at a rate of 16X and a speed of transfers of 115200 bauds.

7. Functionality Tests

A. Optimization

To demonstrate the functioning of the platform it is necessary to begin with the optimization of a modulation in the interface. The selected modulation has nine levels and its waveform is shown in Figure 14 along with the harmonic content which shows the optimization as having a THDv of 7.62%. The shooting angles are shown in the simulation interface in Figure 14.

B. Simulation

In the simulation, physical characteristics of the converter are selected to be implemented as shown in Figure 14. For this test, the selection is the common source sub-topology with asymmetry at the output of 1:3, for which the use of two H bridges is required.

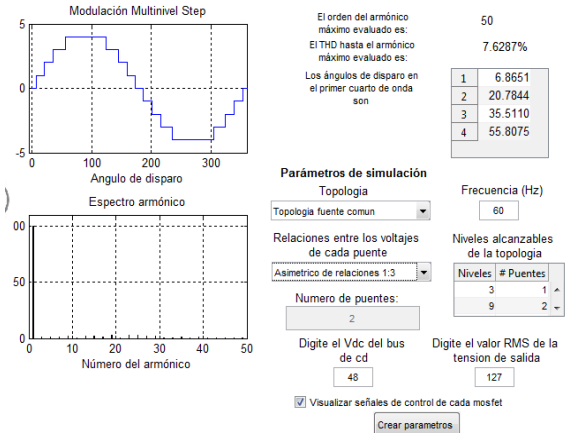

Fig. 14. Simulation interface.

The converter in Simulink is shown in Figure 15, in which one can view the configuration of the hardware.

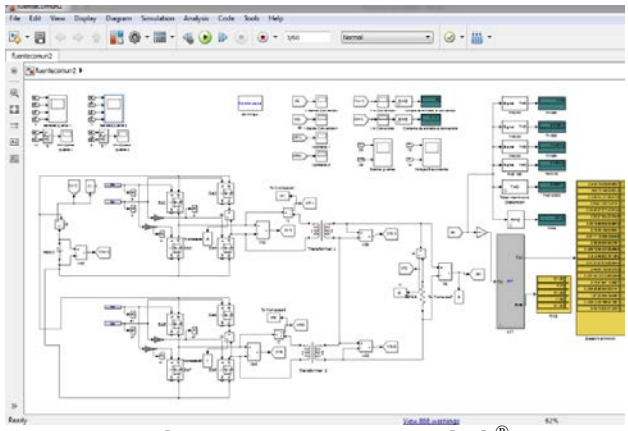

Fig. 15. Simulation converter in Simulink®.

The output of each of the bridges is presented in Figure 16a and the addition of the two that correspond to the output of the multilevel converter simulated in Figure 16b, in which one can observe that it concurs precisely with the theoretical waveform.

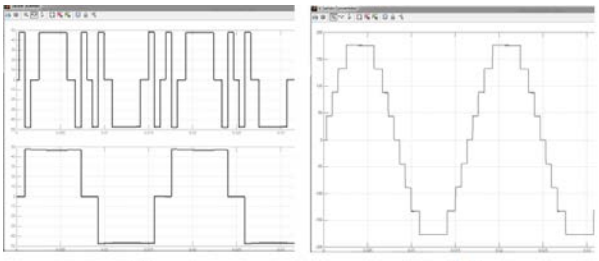

Fig. 16. Output a) Individual H bridges b) Cascaded H. bridges

Implementation of the non-load test

The converter implemented uses only two H-bridges of the platform, each one connected to a transformer at the output. The transformation relationships are of 48/127.2V and of 48/42.42V, calculated in the interface and selected by the second circuit of the switching circuit. In this way, the prototype must be powered by a source of direct current of 48 volts and the result is an alternating voltage waveform with a 170 volt peak. The nominal power of the converter is limited by the design of the transformers, which have a VA of 200. The measurements shown in Figure 15 were made with the Fluke 434 series II network analyzer. The waveform is shown in Figure 17, in which one can note the correspondence of the waveform and the theoretical wavelength.

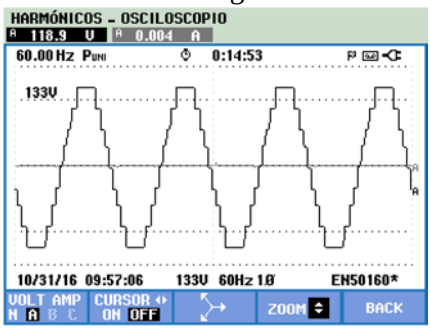

Fig. 17. Step Modulation waveform.

The harmonic spectrum and THDv of the modulation implemented correspond to the theoretical value of the theoretically optimized modulation, as observed in Figure 18.

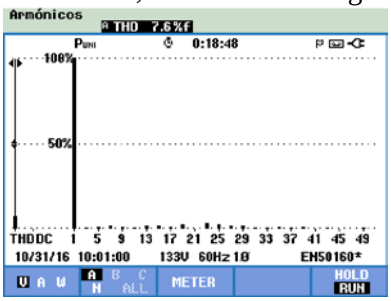

Fig. 18. Harmonic spectrum of the Step modulation.

The non-load test shows that the THDv of the converter's output is exactly equal to the value of the THDv of the theoretically calculated modulation, which validates the correct functioning of the platform, and show its versatility.

Implementation of charge testing

The second test consisted of connecting the converter to a charge of 60W. The waveform is shown in Figure 19.

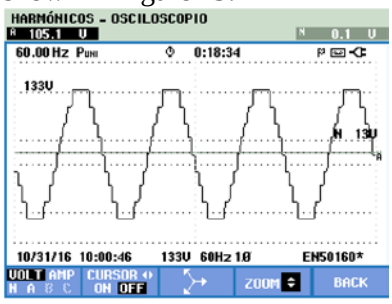

Fig. 19. Step Modulation waveform with load.

DC bus

To acquire the voltage, the Fluke TP 120 sensor was used. For the current waveform, the Fluke 801-

110s sensor was used and via the DAQ card of the *National Instrument* NI6211, the data acquisition software used was Matlab® at a rate of 48 Ksample/s.

In figure 20, one can see the current and DC bus voltage waveforms of each converter using the scalable modulation.

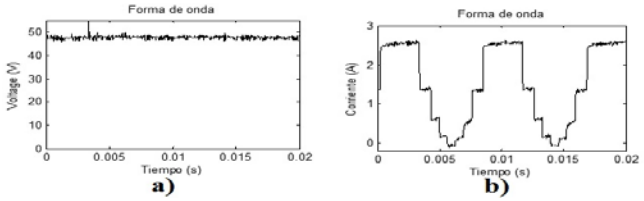

Fig. 20. DC buses with scalable modulation. a) Voltage and b) current of the DC bus of the common source converter

Output variables

The output variables measured are shown in Table 1. The THD of the nine level common source converter along with the power values in order to estimate the efficiency. The result of the non-load test differs subtly from the charge test, in which the THDv increases.

Table I. Table of Experiment Results

Modulation	**Test**	**Parameter**	**Common Source**
Step	Vacuum	RMS Voltage	118.9 V
		THDv	7.8%
	Charge	RMS Voltage	105.1 V
		RMS current	0.571 A
		Output Power	60.01 W
		THDv	7.6%
		THDi	7.6%
		Input Power	70.192 W

The scalable modulation (*step*) demonstrates a greater efficiency due to lower losses as a result of the commutation of the converter.

8. Conclusions

The flexibility of the platform in the research of cascaded multilevel converters permits one to obtain in a matter of seconds the relevant electrical parameters of the common and single source sub-topologies in symmetrical and asymmetrical configurations, validated by a precise implementation in the hardware, thus facilitating the comparison of the sub-topologies' functionalities in terms of energy quality and efficiency.

The THDv obtained in the practice is exactly equal to that which was calculated theoretically, validating the successful functionality of the switching circuits, the system communication, the optimization process, the functioning of the H bridges – in general terms, the adequate functioning of the platform. Considering that the measuring instrument is regulated by the IEEE 519, the THDv is therefore calculated considering the first 50 harmonics, and so the optimization carried out is up to the 50th harmonic and the resulting error is insignificant.

The feasible possibilities of converters with the aim of carrying out a thorough practical study are extremely vast, and they increase with the implementation of PWM modulations. This doubles the number of converters in analyzing their behavior with Step modulations and optimized PWM.

The visual interface facilitates the use of the modular power converter as, in practice; one only has to input the converter's data and closely follow the instructions.

The process of functional optimization and the versatility of creating modulations in a simple way and then implementing them deeply, facilitated by the obtaining of the relevant electronic parameters means that the platform is a powerful tool that aims to analyze, both theoretically and practically, the common and single source sub-topologies in a range of 5 to 81 voltage levels.

For energetic optimization, the implementation of a multi-objective algorithm that doesn't focus the modulations in THD only and includes a criteria of equality in terms of the number of commutations is necessary.

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