INPUT CURRENT SHAPING OF SINGLE PHASE MATRIX CONVERTER BY DESIGNING LC FILTER WITH CLOSED LOOP TECHNIQUE

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Abstract:- This paper presents single phase matrix converter(SPMC) topology capable of generating higher output frequency which is used for high frequency applications such as induction heating. Proposed configuration reduces total harmonic distortion (THD) of supply current with the injection of LC resonant filter at the supply end. By the analysis of dominant side band components of the supply current ,the resonant LC filter is chosen. The cut off frequency of Filter transfer function is estimated through bode plot. However at low output frequency(less than 1kHz) ,filter is only able to reject higher order component, but lower order harmonics mainly 3^{rd} ,5^{th} order components still exist in input current. This demands closed loop control technique for removing lower as well as higher order component simultaneously. Closed loop control of SPMC shapes the input current sinusoidal in nature at low output frequency less than 1Khz but the spike arises for higher output frequency ,which affect the switching stresses. To avoid the spike and make active current shaping, purely sinusoidal, at any output frequency, LC filter is inserted at the supply end. Proper switching technique is explained in detail to eliminate the commutation problem .The simulation results of this topology is verified by using MATLAB/SIMULINK.

Key-Words:- Single phase matrix converter(SPMC),Sinusoidal pulse width modulation(SPWM), Bidirectional switches, Total harmonic distortion(THD), PI controller, Closed loop technique, Resonant Filter.

1. INTRODUCTION

Single phase matrix converter (SPMC) is a type of direct AC-AC converter which has numerous advantages compared to classical dc link converters[1,2,3]. This topology is capable of producing unrestricted output frequency from the supply frequency of 50Hz without use of DC link capacitor[2,4,5] . In addition to this, output voltage magnitude can also be regulated[5]. More attractive features towards this topology includes bidirectional power flow capability and unity input power factor.

The above mentioned advantages, SPMC can be used for many applications, as for examples, induction heating[1,6,7,8]. In case of Induction heating (IH), due to the flow of eddy current (i) through the base of the pot, heat ($i^2 R_{eq}\, t$) is generated. IH consists of inductor-pot ($L_{eq} - R_{eq}$). Now heat is transferred to the pot directly by means of electromagnetic induction. Thus high frequency in the range of 15-100 kHz is required to generate the required magnetic field. Different topologies have already been approached for induction heating [3,8].Conventional method for generation of high frequency requires 2 stages (AC-DC-AC) as shown in figure 1.In between these 2 stages energy storage elements are present which makes system bulky. So by the use of SPMC topology it is possible to generate higher frequency directly with and without regulating the output voltage. As this paper aims at application mainly in case of high frequency appliances, particularly, induction heating, so high THD coming at the load end will not deteriorate the system instead it enhances the heating.

However demerit of this converter is high THD at the supply current which will impair the utility. As a result there is a chance of power quality pollution. So main emphasis of this paper is active input current shaping .This

paper represents open loop analysis of SPMC to decide the cause of increase in harmonics. Then LC filter is used at the supply end in case of open loop for mitigation of harmonics. Secondly due to some disadvantages still appear after filtering, closed loop control technique is employed here. At high output frequency, spikes may be developed which will be avoided by the implementation of LC filter in closed loop technique. Another disadvantage of this converter is absence of freewheeling path which makes load current discontinuous. So to avoid commutation problem proper switching techniques are applied.

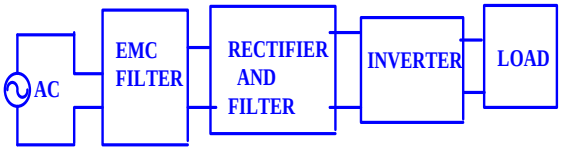


Fig. 1. Classical 2stage AC-AC converter

2. Problem Formulation In The Proposed SPMC Topology

SPMC consists of 4 bidirectional switches as shown in figure 2[2,4,5]. By the use of these bidirectional switches this converter is capable of conducting current in both directions and also able to block both forward and reverse voltage. So combination of IGBT and diode are used to construct a single bidirectional switch[9]. From various types of bidirectional switch topology, conventionally common emitter configuration is preferred as shown in figure 2.1 [9]. IGBT is generally used for high power applications which has high switching speed and current carrying capability. Diode is favored due to high reverse voltage blocking capability. Presence of more numbers of bidirectional switches may be overcome by absence of dc link capacitor in case of SPMC[10]. But disadvantage of this converter is lack of freewheeling path[11] .This topology allows fixed turn on and off of the switches within 1cycle of supply frequency for the required output frequency. For example if output frequency is of 100Hz, then 4 times switching sequence occur within 1 cycle of supply frequency(50Hz).Due to this finite switching sequence it is not easy to commute current from one switching sequence to another without preventing load current. Another drawback happens due to the turn off characteristics of IGBT which makes switching sequence non spontaneous. It is due to tailing of collector current which makes short circuit with next switching sequence[12,13].So to avoid above mentioned shortcomings a proper switching sequence is needed which not only avoids commutation problem but also provides continuous load current.

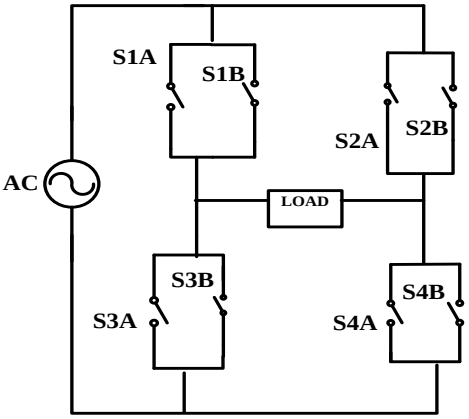


Fig. 2: SPMC topology

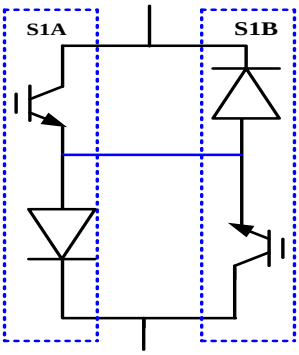


Fig. 2.1.Common Emitter Bidirectional Switch

2.1. Elimination of Commutation problem

This topology is used to generate any output frequency from the supply frequency of 50Hz by the use of 4 modes given below in figure 2.2-2.5and in Table 1[2]. But proper switching technique is needed to produce the required output frequency[14]. This converter adheres to some principles. If both incoming and outgoing switches are turn on or off at same time then there is a chance of over-current and over-voltage respectively. So SPMC is acting on the basis that only 1 of the 2 switches should be on at any time as shown in figure 2.2-2.5. This switching technique not only ensures prevention of short circuit of power

supply but also provides uninterrupted load current. The modulation task of SPMC is to distribute the time in such a manner that each output terminal is connected to an input phase so that sinusoidal current drawn from the supply with unity power factor. The commutation scheme claims for continuous load current during dead time[12,13]. So safe switching operation is needed whose objective is to activate only conducting devices at any point of time.

Table I(Mode Of Operation)

	Positive half cycle		Negative half cycle	
Mode of operation	Forward power flow	Reverse power flow	Forward power flow	Reverse power flow
Current Path	Supply-S1A-Load-S4A-Supply.	Supply - S2A-Load - S3A-supply.	Supply-S3B-Load-S2B-Supply	Supply-S4B – Load-S1B-Supply.
Commutation switch	S1A, S2B	S1B S2A	S3B S4A	S4B S3A
PWM switch	S4A	S3A	S2B	S1B

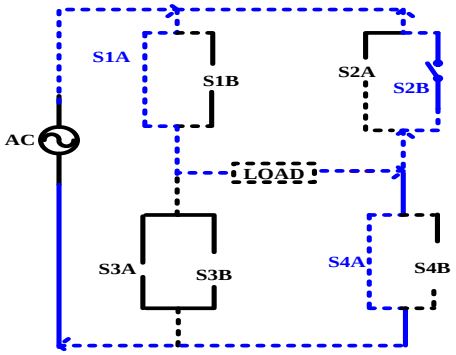


Fig.2.2.Forward power flow(positive cycle)

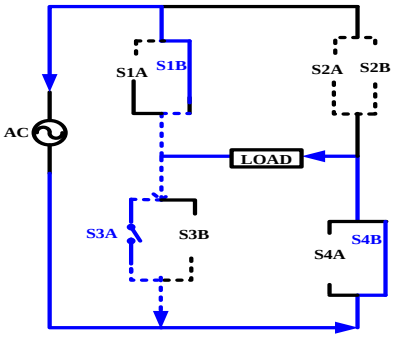


Fig. 2.3. Reverse power flow (negative cycle)

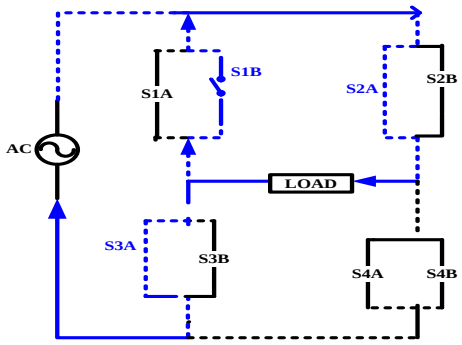


Fig. 2.4. Reverse power flow (positive cycle)

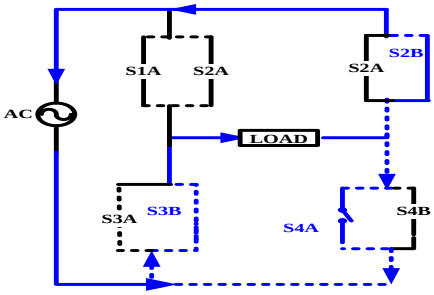


Fig. 2.5. Forward power flow (negative cycle)

If output and input frequency are of 50Hz only 2 modes come into consideration as given in TABLE 2. During 1st interval ,current flows through S1A and S4A. Here S4A acts as a PWM switch. When S4A is turned off due to high switching frequency as shown in figure 2.6, to make load current continuous, power flows through S2B. So S1A acts in conjunction with S2B for commutation purpose. Similarly for negative half cycle S4B, S3A are used as a commutation switch and S1B as a PWM switch. With the help of all the 4 modes, SPMC is able to generate any output frequency only with the help of proper switching sequence given in Table 2.

Table 2 (SWITCHING SEQUENCE)

Freq. (Hz)		Interval	Switch behavior	
			PWM	Commutation
I/P	O/P			
50	50	1	S4A	S1A S2A
		2	S1B	S4B S3A
	100	1	S4A	S1A S2B
		2	S3A	S2A S1B
		3	S2B	S3B S4A
		4	S1B	S4B S3A

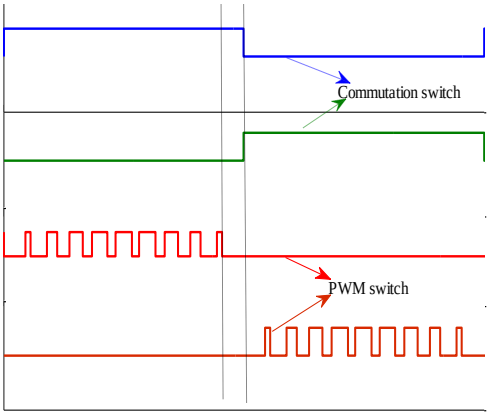


Fig. 2.6. (Switching arrangement during f_{out} =50Hz)

3. Input Current Harmonic Problem

Crucial problem of this topology is THD of supply current coming very high[15]. Due to rise in harmonics at the supply end, utility will be affected .Real cause of increase in harmonics is high switching frequency which will create quasi square wave inside the sinusoidal envelope of supply current as shown in figure 3.Though input current is in phase with supply voltage but due to the presence of higher percentage of side band components, power quality will be degraded. These components are highest at switching frequency. Apart from switching frequency (f_{sw}) sub harmonic also located at $f_{sw} \pm f_{out}$ (where f_{out} output frequency) , 3rd (150Hz), 5th (250Hz) component. Firstly dependency of side band component with switching frequency (f_{sw}) and output frequency(f_{out}) are analyzed in detail in case of open loop .

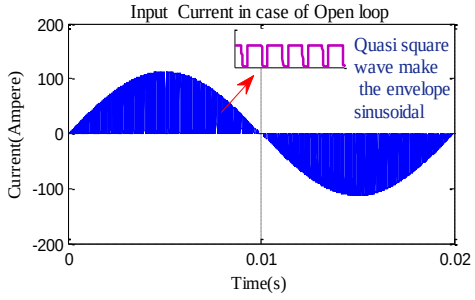


Fig. 3.Input current waveform with presence of ripple

3.1. Open Loop Analysis And Simulation Result

Harmonic enter into the system due to side band components. Mainly supply current contains higher percentage of dominant side band component at switching frequency for any range of output frequency. In addition to switching frequency, sub harmonics also located at multiple of output frequency, $f_{sw} \pm f_{out}$ (where f_{sw} , f_{out} represent switching and output frequency respectively).But lower order components are negligible in percentage .These things are analyzed from simulation result shown below.

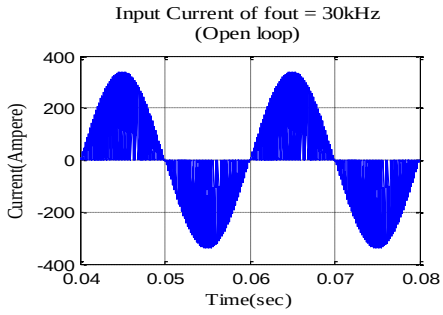


Fig. 4.1. Input current for $f_{out} = 30kHz$

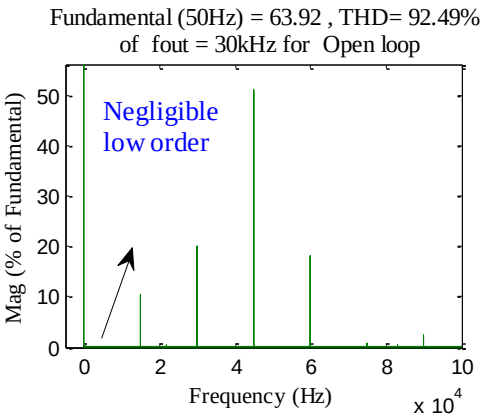


Fig. 4.2. Input current FFT for $f_{out} = 30kHz$

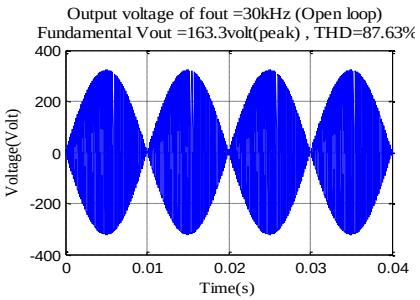


Fig. 4.3. Output Voltage of $f_{out} = 30kHz$

IH required high frequency mentioned above (30kHz taken here for analysis), load voltage THD coming high (%) will not affect the system badly as shown in figure 4.3. But THD of supply current which is coming very high i.e. of 92.49% will degrade the power quality as shown in figure 4.1. It is clear from FFT analysis that, higher percentage of harmonic is due to side band component, which is highest at switching frequency (= 45kHz) of 51.12%. It also contains 20%, 18% side band component at 30kHz,60KHz respectively as given in figure 4.2 .But it is clearly visible from FFT analysis that lower order component is completely neglected i.e. up to 15kHz whose side band value is of 10%. Obviously low order components are complely neglected.

Similarly for output frequency of 5kHz ,it is found from figure that THD of 102.19% mainly due to switching frequency component which is of 51% and second dominant component 31% is at 10kHz as shown in fig. 4.4.

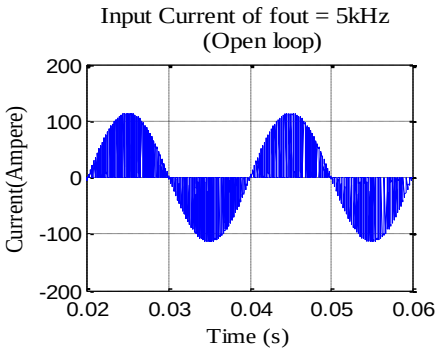


Fig. 4.4 Input current waveform for $f_{out} = 5kHz$

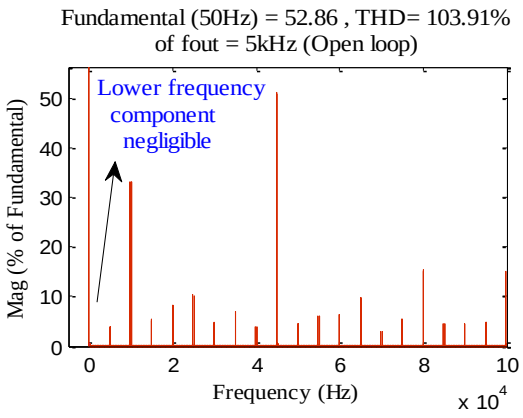


Fig. 4.5. Input current FFT of $f_{out} = 5kHz$

It is concluded that for higher output frequency dominant component is neglected for lower order. Thus rejection of only higher order component is needed for reduction of harmonics.

Further for low level of output frequency (50Hz,100Hz,150Hz), in addition to switching frequency dominant sub harmonic components still exist for lower order i.e. at 150Hz(3rd order), 250Hz(5th order),350Hz(7th order) which is clearly visible from extended FFT analysis as shown below.

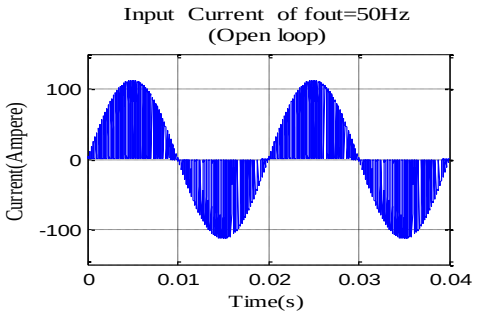


Fig. 4.6. Input current of $f_{out} = 50Hz$

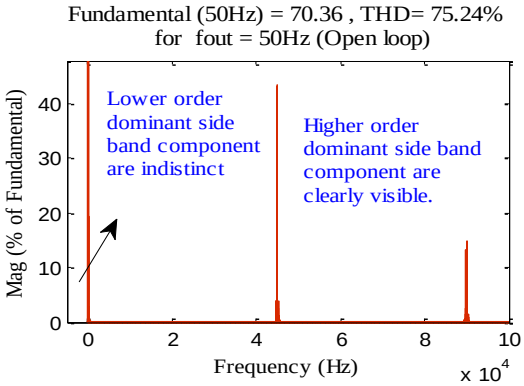


Fig. 4.7. Overall Input current FFT of $f_{out} = 50Hz$

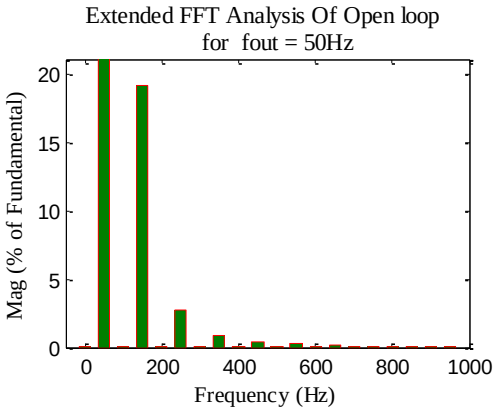


Fig.4.8. Input current extended FFT analysis for $f_{out} = 50Hz$

In case of output frequency 50Hz as shown in figure 4.6 THD of supply current coming 75.24% which is mainly because of the highest side band component at switching frequency visible from overall FFT analysis as shown in figure 4.7. But presence of lower order components are not distinguishable from this figure 4.7. So extended FFT analysis as shown in figure 4.8 gives idea about presence of dominant side band component at 3rd order (150Hz) i.e. of 19.25%.

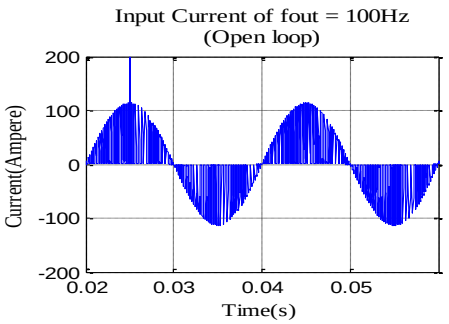


Fig. 4.9. Input current waveform for $f_{out} = 100Hz$

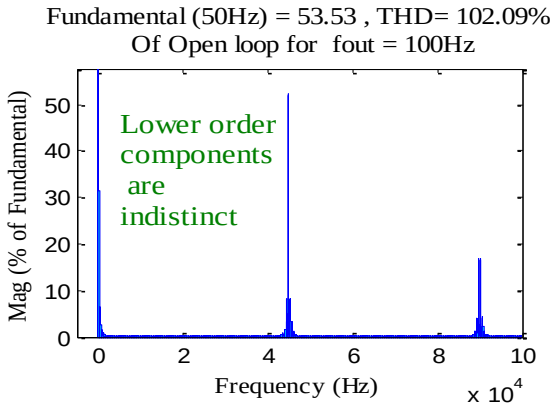


Fig. 4.10. Overall Input current FFT for $f_{out} = 100Hz$

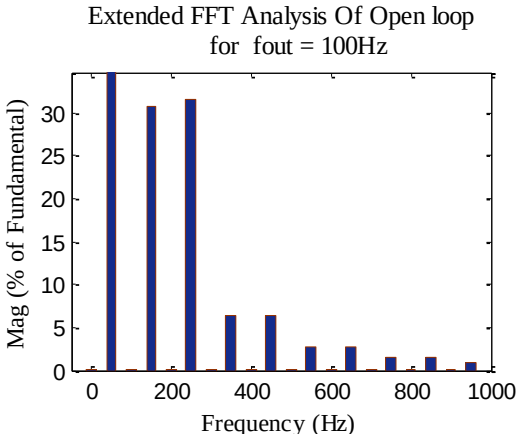


Fig. 4.11. Input current extended FFT analysis for $f_{out} = 100Hz$

Again for output frequency of 100Hz, THD of 102.09% , mainly due to switching frequency(45kHz) of 52% are visible from figure 4.10 .Also highest dominant components are of 31%, 33% present at 3rd (150Hz),5th (250Hz) component respectively as shown in fig 4.11 .

Thus It is finalized that, for lower output frequency dominant component is present for lower order.

3.2. INPUT CURRENT SHAPING

For input current shaping LC resonant filter is inserted to filter out high frequency current component entering into the supply end . If RL low pass filter injected instead of LC filter, then there is chance of power loss(i^2R). Consequently efficiency decreases.

But by the use of LC resonant filter these shortcomings will be eliminated as it will not affect power level. To calculate filter parameters cutoff frequency plays a vital role. Filter parameters are estimated in such a way that it will not affect amplitude of output voltage or current and input current. From previous analysis it is observed that harmonics enter into the system due to side band component. Thus for current shaping these components should be rejected. So cut off frequency should be selected in such a way that it will reject all high order components and passes through low frequency component. For output frequency ranging above 5kHz, higher percentage of component which greatly enhance overall harmonics starting from 10kHz with complete negligence of low order component as discussed above . Due to this if cutoff frequency less than 5kHz is chosen, then it will reject all high order side band content and make input current ripple free.

To find out cutoff frequency transfer function of the filter should be find out as shown in fig.5. By applying voltage divider rule to find out the output voltage of the filter (V_f) and taking Laplace transform ,the transfer function becomes

$$\text{Transfer function} = \frac{V_f(s)}{V_i(s)} = \frac{1/Cs}{Ls + 1/Cs}$$

$$\frac{V_f(s)}{V_i(s)} = \frac{1/CL}{s^2 + 1/CL}$$

$$\omega \text{ (cutoff frequency)} = \frac{1}{\sqrt{CL}}$$

$$\text{It is expressed in terms of } \frac{\text{radian}}{\text{sec}}$$

As power consumption before and after filtering remain unchanged , current transfer function become reciprocal of voltage transfer function as shown below. Main focus of this paper is to reduce ripple which exist inside the sinusoidal envelope of source current by making it purely sinusoidal as shown in figure. So current transfer function plays important role. As shaping of current before filtering (I_i) is needed, so that is treated as a output end to calculate current transfer function.

$$\text{Power before filtering } (V_i I_i) = \text{Power after filtering} (V_f I_f)$$

$$\text{Transfer function} = \frac{I_i(s)}{I_f(s)} = \frac{1/CL}{s^2 + 1/CL}$$

From the open loop analysis, it is seen that output frequency ranging above 5kHz, harmonics are more dominant at switching frequency (=45kHz) and beyond the output frequency . Thus it is easy to attenuate higher order harmonics by choosing proper cutoff frequency with the help of LC resonant filter . As all the dominant components are started after 5kHz so that for the output frequency ranging above 5kHz , 3.063kHz is taken as cutoff frequency.

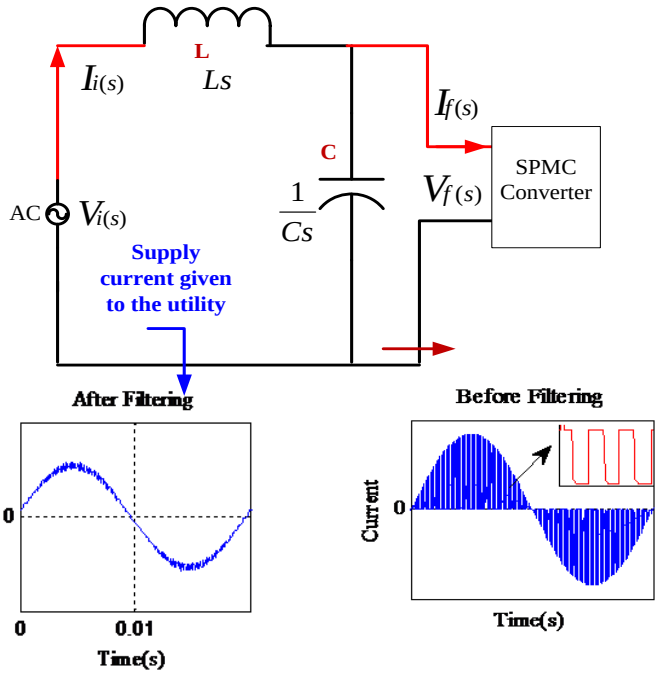
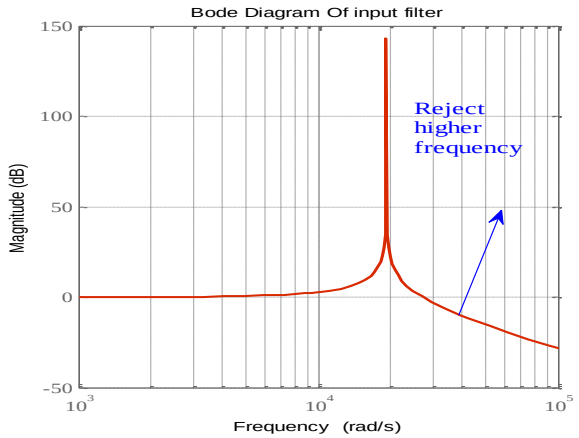


Fig. 3. LC resonant filter

Fig. 5.1. Bode plot



Transfer function plays a vital role to draw the bode diagram as shown above in figure 5.1, which confirms rejection of higher order harmonics.

3.2.1. Open loop with LC filter and Simulation Result

By the insertion of LC filter at the supply end harmonic reduces as discussed below.

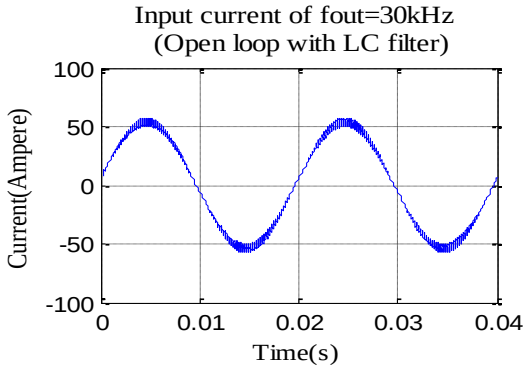


Fig. 6.1. Input current at $f_{out} = 30kHz$

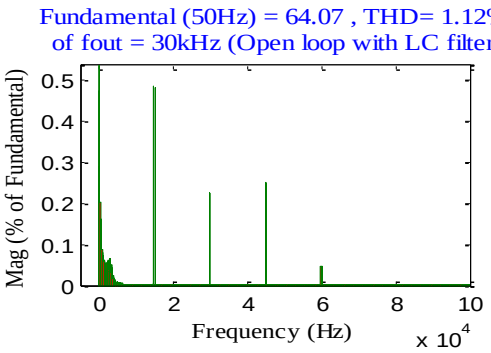


Fig. 6.2. Input current THD for $f_{out} = 30kHz$

It is seen from FFT analysis of output frequency 30kHz that dominant side band component being present at switching frequency of 45kHz which is completely neglected .Also sub harmonics are completely mitigated by making overall THD 1.12% as mentioned in figure 6.3. So Current wave form become ripple free as shown in figure 6.1. It is also observed that filter parameters are adjusted in such a way that amplitude after and before filtering remains almost same 64.07 ampere. Though output voltage as shown in figure 6.2 contain higher percentage of harmonics but it is useful for IH.

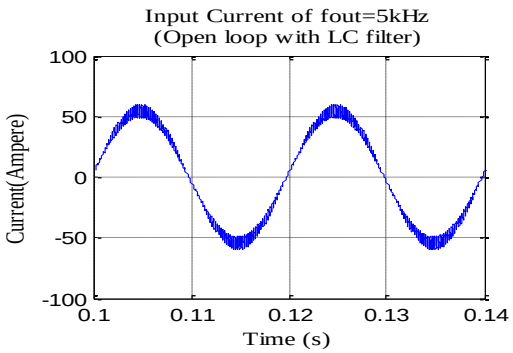


Fig. 6.3. Input current at $f_{out} = 5kHz$

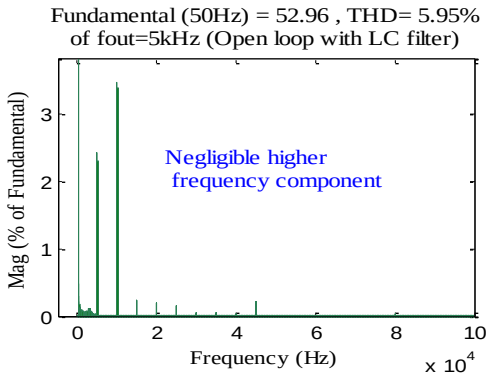


Fig. 6.4. Input current THD for $f_{out} = 5kHz$

Similarly for output frequency of 5kHz harmonic distortion 5.95% coming by rejecting all side band components.

So it is cleared that for higher output frequency ,normally dominant side band components arises from very high order of supply frequency(50Hz) and negligible lower order component . Thus it is easy to select cut off frequency to reject higher order component. As a result for higher level of output frequency (above 1kHz) harmonics mitigation take place properly.

But in case of low output frequency level(50Hz, 100 Hz,150Hz) , dominant side band components present in addition to switching frequency(45kHz) also at 3^{rd} ,5^{th} etc harmonics as discussed above. So to reject side band component if same cutoff frequency(3.062kHz) value is chosen, then highest order side band component neglected completely as shown in figure. But still 3^{rd} harmonic presence make the waveform distorted as shown in fig. If cutoff frequency less than 3^{rd} harmonic (150 Hz)is selected to reject this component, output waveform is affected. Apart from output waveform, input current are not in phase with input voltage.

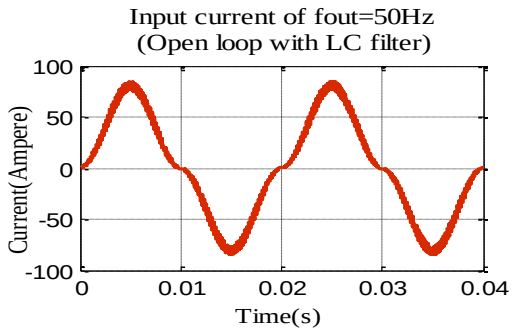


Fig. 6.5 . Input current THD for f_{out} = **50**Hz

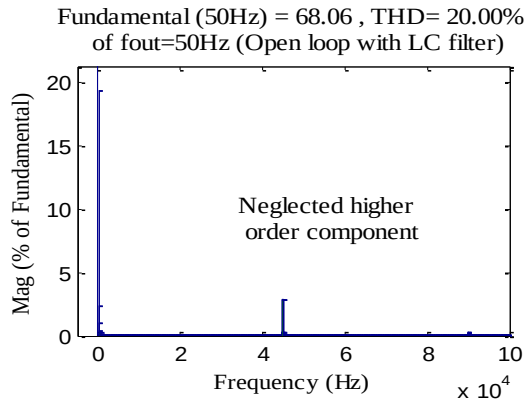


Fig. 6.6. Input current THD for f_{out} = $50Hz$

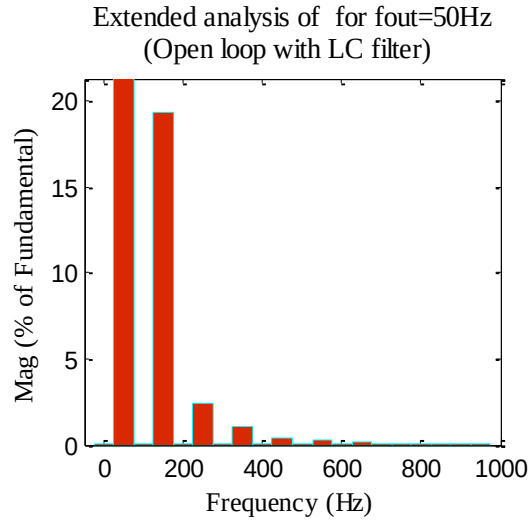


Fig. 6.7. Input current THD for f_{out} = **50**Hz

From FFT analysis of output frequency 50Hz,it is clear that though higher order component completely neglected, but overall THD is still coming 20% as given in fig.6.6 This is mainly due to 3rd order component which is of 19.29% as shown in fig.6.7 .

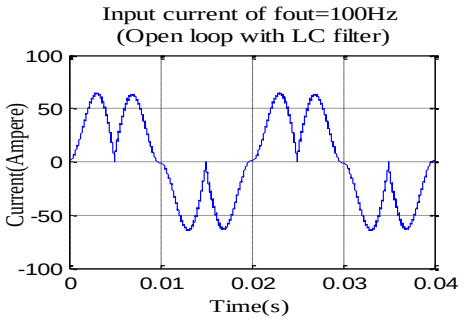


Fig. 6.8. Input Current for f_{out} = $100Hz$

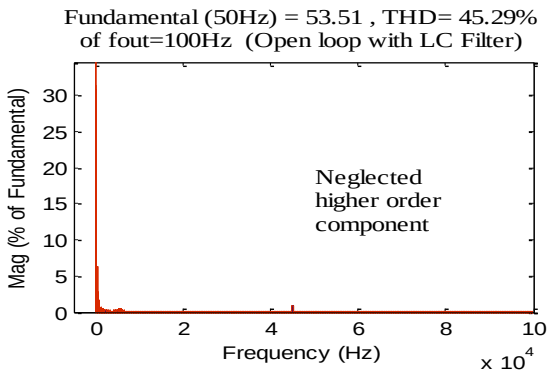


Fig. 6.9. Input Current THD for f_{out} = $100Hz$

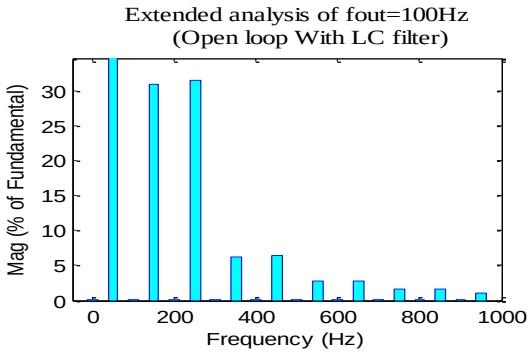


Fig. 6.10. Extended FFT for f_{out} = $100Hz$

Similarly for output frequency of 100Hz as shown above in figure 6.8-6.10,it is cleared that after filtering, due to the presence of 3rd ,5th component current wave form resonate twice within 1cycle of supply frequency. This 2 components will make overall THD 45.23%.

Thus it is finalized that for low level of output frequency it is difficult to choose the cutoff frequency properly. Though highest side band component which is present at switching frequency completely neglected by the use of filtering but still low order component mitigation cannot take place properly.

3.2.2.CLOSED LOOP TECHNIQUE

Current control closed loop operation is applied here to overcome above mentioned shortcomings. For operation of closed loop as shown in figure 7 supply current is being tapped from input supply and being compared to the reference sinusoidal signal. The error signal now passes through PI controller and used to do correction of the error. Due to this input current is corrected by mitigation of ripple. To implement AC-AC SPMC, closed loop current control techniques are able to produce SPWM for the operation of the switches. The output of PI controller is the required modulating signal. This is compared with carrier signal (which decides switching frequency) to produce pulse .

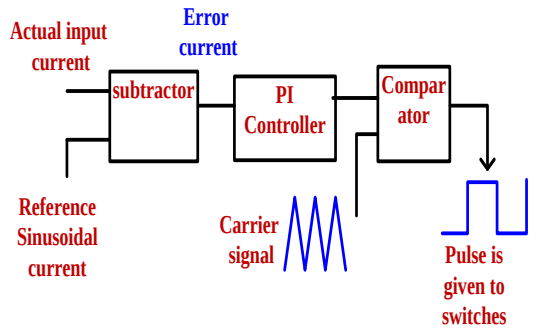


Fig. 7. Closed loop technique

3.2.2.1. Simulation result Of Closed loop without Filter

By the use of closed loop technique all dominant side band components are reduced and make the input current ripple free as discussed below.

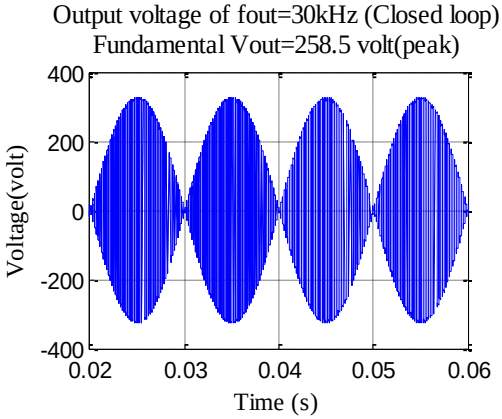


Fig. 8.1.Output Voltage for $f_{out} = 30kHz$

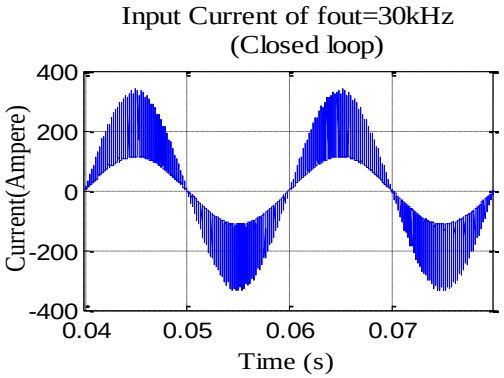


Fig. 8.2.Input Current for $f_{out} = 30kHz$

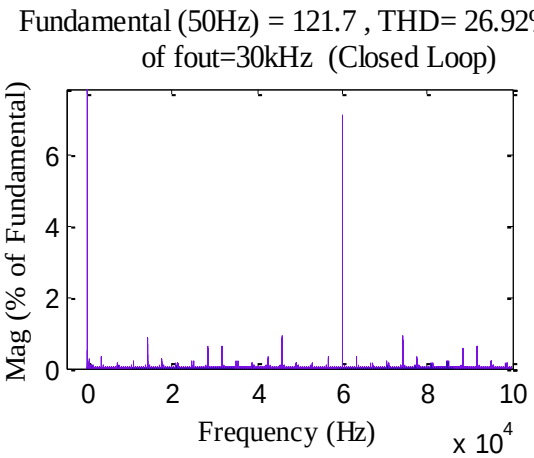


Fig. 8.3.Input Current FFT for $f_{out} = 30kHz$

It is observed that in case of output frequency of 30kHz input current ripple reduces as shown in fig 8.2.Though side band component percentage reduces to very low level(less than 10%) as shown in figure 8.3, but THD is coming 26.92%.It is due to presence of spike. It is also observed that Fundamental output voltage and input current amplitude rises in comparison to open loop.

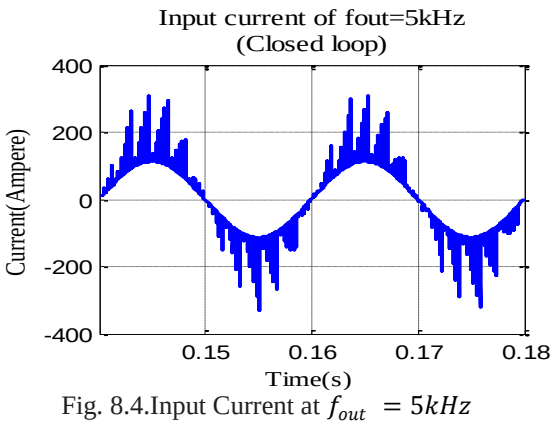


Fig. 8.4.Input Current at $f_{out} = 5kHz$

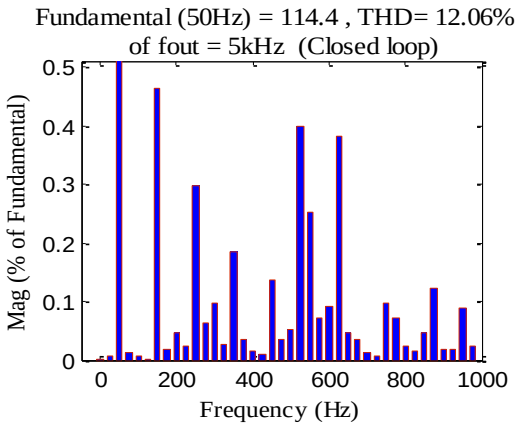


Fig. 8.5.Input Current THD at $f_{out} = 5kHz$

Similarly it is seen that, spike also exists in the current waveform in case of output frequency of 5kHz as shown in figure 8.4.Reduction of side band component is also clearly visible from FFT analysis as shown in figure 8.5.So overall THD become 12.06% which is mainly due to spike .

But due to the application in case of induction heating , high frequency is required. It is seen that in case of this frequency range though side band component reduces but spike arises which will affect the switches.

In case of lower output frequency range all the above discussed shortcomings in case of open loop analysis are avoided by the use of closed loop technique as discussed below.

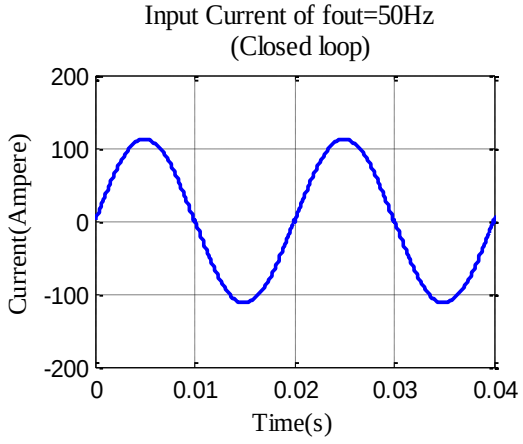


Fig. 8.6..Input Current at $f_{out} = 50Hz$

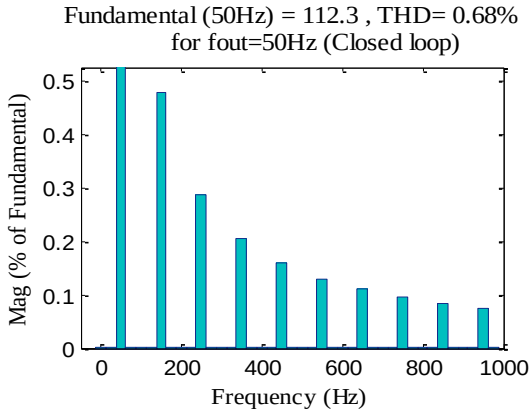


Fig. 8.7.Input Current THD at $f_{out} = 50Hz$

In case of output frequency 50Hz as shown in figure 8.6 it is seen that input current coming purely sinusoidal. It is due to elimination of all side band component as shown in figure 8.7.So that overall THD become 0.68% with increase in magnitude of fundamental voltage

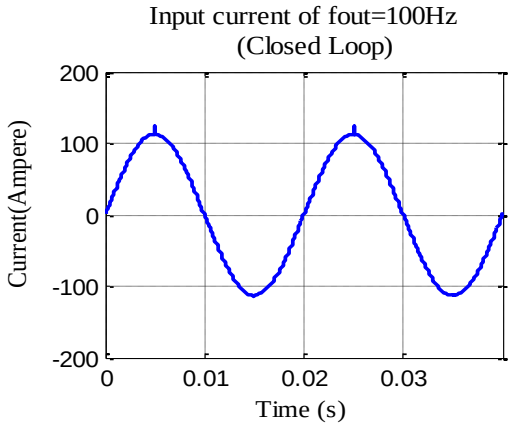


Fig. 8.8..Input Current at $f_{out} = 100Hz$

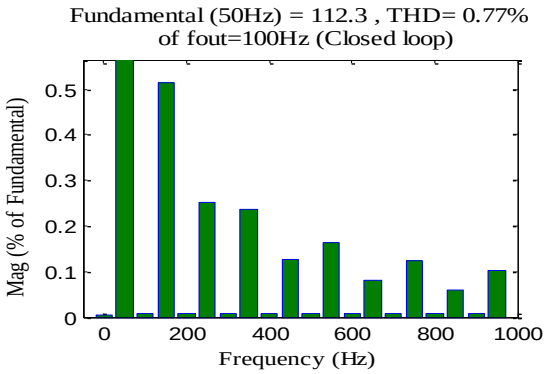


Fig. 8.9.Input Current THD at $f_{out} = 100Hz$

Similarly in case of output frequency 100Hz, it is seen that input current become ripple free and overall THD become 0.68% as shown in figure 8.8 and 8.9.

Thus it is finalized that for the range of low output frequency, input current coming purely sinusoidal with extremely less percentage of THD with no further problem.

3.2.2.2. CLOSED LOOP WITH LC FILTER

Though harmonic reduces by closed loop analysis but due to the presence of spike as shown in fig 8.2, 8.4 switches may be affected badly. In order to reduce spike LC filter is inserted in conjunction with closed loop control technique. Cut off frequency selection is not required here. So the shortcomings which arise during open loop with filter analysis for the choice of cut off frequency will be avoided. Here LC filter is used to force the supply current to follow the reference current .So it will have sinusoidal current by elimination of ripple and spike with unity power factor.

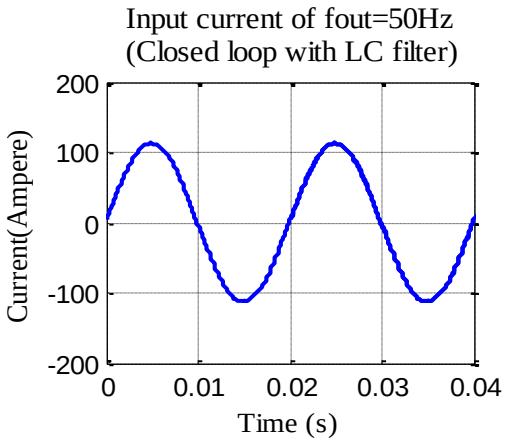


Fig. 9.1.Input current for $f_{out} = 50Hz$

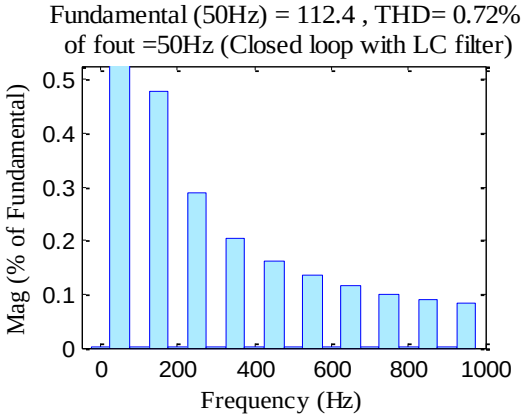


Fig. 9.2. Input current FFT for $f_{out} = 50Hz$

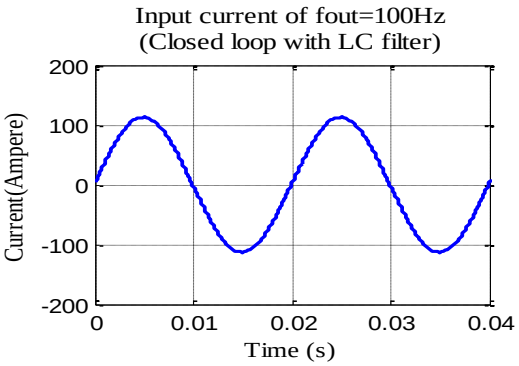


Fig. 9.3. Input current for $f_{out} = 100Hz$

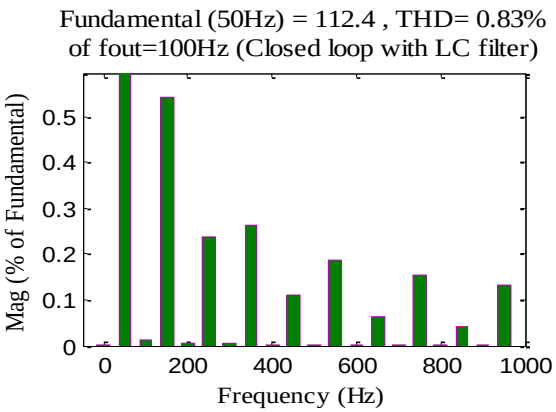


Fig. 9.4. Input current FFT for $f_{out} = 100Hz$

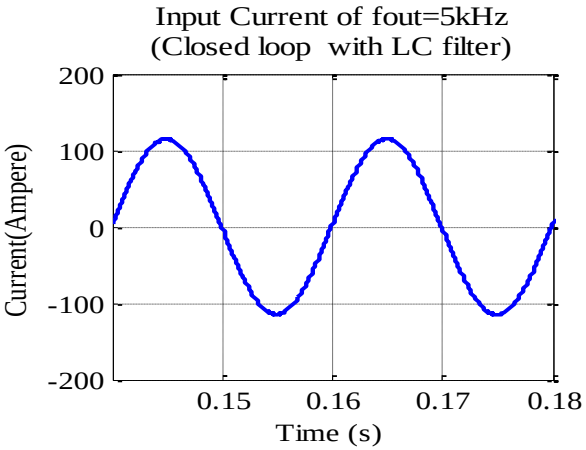


Fig. 9.5. Input current for $f_{out} = 5kHz$

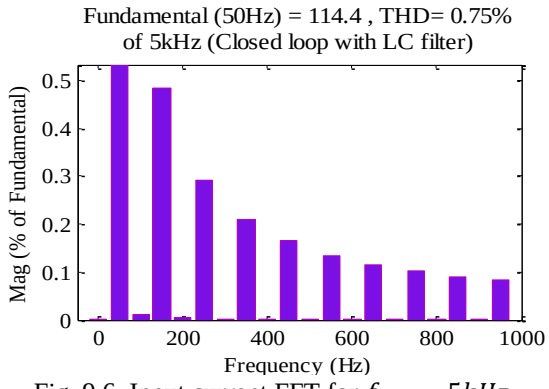


Fig. 9.6. Input current FFT for $f_{out} = 5kHz$

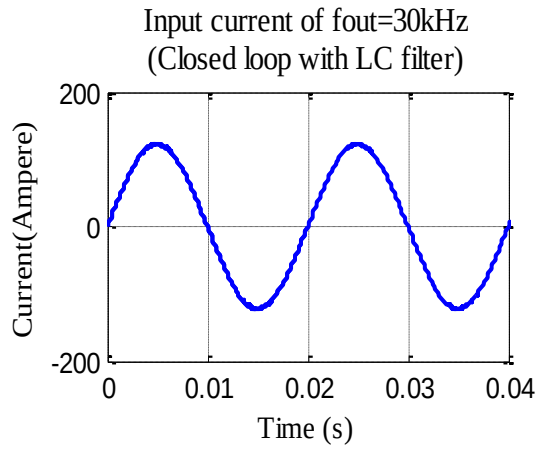


Fig. 9.7. Input current for $f_{out} = 30kHz$

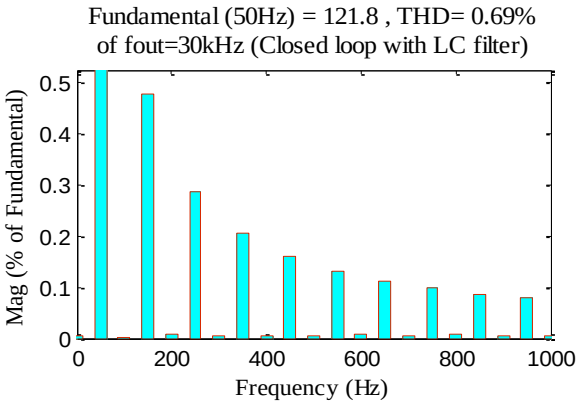


Fig. 9.7. Input current for $f_{out} = 30kHz$

All the ripple present inside the envelope are completely mitigated as shown in above analysis . It is visible from waveform and FFT analysis of all the range of output frequency as shown in figure 9.1-9.7 .Dominant side band component completely neglected by making ripple free current waveform.

4. RESULT DISUSSION OF BOTH OPEN LOOP AND CLOSED LOOP ANLYSIS

A comparison is carried out between a simulation of SPMC with open loop and closed loop technique given above in tabular form.

Table 3 Open loop (Input current THD analysis)

O/p Freq. (Hz)	W/O filter		With filter	
	THD (in %)	Remarks for dominant side band component	THD (in %)	Remarks for dominant side band component
50	75.24	Switching freq.(45kHz) =43% 150Hz =19.24%	20	Rejection of all component. Only 150Hz(3rd order) = 19.39% exist
100	102.09	Switching freq.(45kHz) =52% 150Hz=30.79 % 250Hz =31.93%	45.29	Rejection of all component. Only 150Hz(3rd order) = 30% ,250Hz(5th order) =31% exist
5k	103.91	switching freq.(45kHz) =51% 10kHz=33% 80kHz=15%	5.99	Rejection of all Component
30k	92.49	switching freq.(45kHz) =51% 30kHz=20% 60kHz=18%	1.03	Rejection of all Component

From this tabulation presence of side band component analyzed first. Then with injection of filter reduction in THD and side band component for all the frequency are discussed clearly. But it is seen that in case of 50Hz, 100Hz output frequency still dominant component exist.

Table 4 Closed loop (Input current THD analysis)

O/P Freq. (Hz)	W/O filter		With filter	
	THD (in %)	Remarks for dominant component	THD (in %)	Remarks for dominant component
50	0.68	Rejection of all component	0.72	Rejection of all Component
100	0.77	Rejection of all component	0.83	Rejection of all Component
5k	12.06	Rejection of all Component but presence of spike increase THD.	0.75	Rejection of all Component
30k	26.92	Rejection of all component but presence of spike increase THD.	0.69	Rejection of all Component

To overcome disadvantages in case of lower frequency level as shown in table 3, closed loop technique employed.. It is clear from above Table 4 is that THD reduces to negligible percentage in case of 50HZ and 100Hz.But due to presence of spike THD rises in case of 5kHz and 30kHz frequency. So better result analyzed from closed loop with filter as shown in Table 4.

Table 5 Open loop(Input current and output voltage Fundamental and output THD analysis)

Signal Analysis \ O/P Freq. (Hz)		50	100	5k	30k
Input Current (Ampere)	Without filter	70.36	53.53	52.86	63.91
	With filter	68.06	53.51	52.96	64.09
Output Voltage (volt)	Without filter	200.3	160.3	149.9	163.3
	With filter	194.8	160.3	149.8	163.4
Output Voltage THD (in %)	Without filter	74.96	91.66	97.82	87.63
	With filter	79.12	92.06	98.16	87.75

It is seen that amplitude of output voltage and current and input current remain unaltered even after filtering. So filter parameters plays vital role.

Table 6 Closed loop(Input current and Output voltage Fundamental and output THD analysis)

Signal Analysis \ O/P Freq.(Hz)		50	100	5k	30k
Input Current (Ampere)	Without filter	112.3	112.4	114.3	121.7
	With filter	112.4	112.4	114.4	121.8
Output Voltage (volt)	Without filter	319.9	270.9	258.5	258.5
	With filter	320.1	271	258.5	258.5
Output Voltage THD (in %)	Without filter	0.70	62.85	64.11	64.22
	With filter	0.67	62.84	63.97	63.96

From the simulation result given in above Table, it is seen that output voltage and input current fundamental has been stepped up after compensation. For example in case of output frequency 30kHz, output voltage has been rises from 163.3 volt(peak) to 258.5 volt(peak) which contribute to 58.29% increase. Similarly input current fundamental is 90.42% increased. Further supply current THD has been reduced completely with the help of closed loop compensation .

5. Conclusion

In this paper, operation and closed loop simulation of SPMC has been explained in detail. This topology replaces 2 stage classical converter (AC-DC-AC) for generation of high frequency directly without need of energy storage element. Thus lack of energy storage element will enhance the efficiency level. So this converter is more applicable for high frequency applications, such as, induction heating. With the help of proper switching sequences elimination of commutation takes place, so that load current flow continuously. Due to rise in dominant side band component at the supply end ,THD of input current rises which has adverse effect on power quality . At first, dependency of side band component with switching frequency and output frequency are analyzed in detail in case of open loop .Then to make the topology noiseless, elimination of dominant side band components are needed. So that, LC resonant filter is inserted at the supply end. By the selection of proper cut off frequency, filter parameters are estimated and which helps to reject all higher order harmonics. But it is seen that for low level of output frequency, it is difficult to attenuate the 3^{rd} ,5^{th} order components .To avoid above mentioned shortcomings, closed loop technique with PI controller is employed . Though this closed loop method reduces the harmonics but still spike arises in case of higher output frequency level, which increases the switching stresses. Closed loop with LC filter at the supply end overcomes the above spike and stress problems.

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