

Performance Analysis of 20 nm Pentagonal and Trapezoidal NanoWire Transistor with Si and Ge Channel

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Abstract: - In this paper, we have analyzed the variability in the performance of Gate All Around Nanowire Field Effect Transistor (GAA NWFET) due to their cross sectional shapes, channel diameter, channel height and channel material with the aid of 3D Technology Computer Aided Design (TCAD) simulations. Pentagonal and trapezoidal Cross sectional shapes have been designed for Si and Ge based channel with different values of diameter and heights. The performance is evaluated in terms of I_{on} current, switching speed, leakage current, transfer and output characteristics, Subthreshold Swing (SS), Drain Induced Barrier Lowering (DIBL), threshold voltage (V_{th}) and compared with triangular NWT. After comparison, it shows that Si Pentagonal NWT structure is showing better performance i.e. high on-current, low DIBL and low SS. Ge NWT offers better leakage current.

Key-Words: - GAA FET; TCAD; NWT; DIBL; SS; Threshold Voltage.

1 Introduction

With the shrinkage in technology, no. of transistors is continuously increasing in an IC. Therefore, the transistors have to be downscaled, but making transistors smaller leads to degradation in device performance [1]. This degradation is due to dominant short channel effects such as subthreshold swing, drain induced barrier lowering, threshold voltage (V_{th}) etc. Several structures like double gate MOSFET (DG MOSFET) [2], tri-gate MOSFET (TG MOSFET) [3] have emerged as an alternative of MOSFETs. After DG MOSFET, gate all around (GAA) structures have the advantages of strong electrostatic control of channel by gate [4]. The triangular, rectangular and circular NWTs have been discussed in the literature [5].

Semiconductor NW is an evolutionary technology as a powerful materials that are used in controlled growth and organizations [6], which is making it dominating technology of nano scaled electronics. Now a days, there is great interest in synthesis and characterization of one Dimensional (1D) structures like nanotubes, NWs, nanobelts and nanorods. Inorganic NWs have a higher conducting and higher electrical properties. NWs have smallest dimension for efficient exciton and transport of electrons. A NW structure is an object with 1D aspect in which

the length to width ratio is greater than 10 and possible width is less than 10 nm. Electrical conductivity of NW is also affected by structural defect, reduces impurity and its dimensions like cross sectional area, corner effects etc.

2 GAA NWFET

GAA NWFETs are allowed to sustain the relentless progress in CMOS scaling. NWFETs can be formed in high yield with repeated and reproducible electronics properties as required for CMOS technology [7]. Second, the channel diameter can be kept below 10nm without compromising its electrical performance. In addition, the smooth surface, crystalline structure and the ability of axial and radial NW hetrostructures can suppress the charge scattering. Use of very small dimensions (in nm) causes small mean free path of electron which enhance the drift velocity of electron in channel and depicts higher mobility [8]. Fig. 1 shows Nanowire FETs.

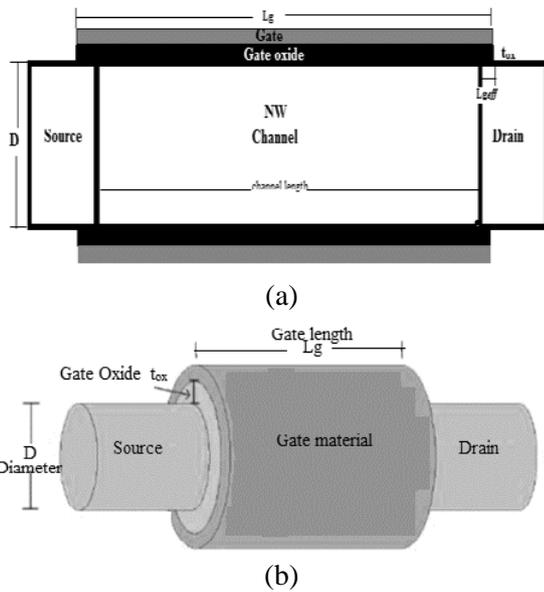


Fig.1 (a) Schematic 2D representation of GAA NWFET, (b) Schematic 3D representation of CNWFET.

2.1 SiNWFET

SiNWFETs are getting more attraction because of their better electrostatic integrity, excellent conductivity, less scattering and higher mobility even at nano scale. Various types of SiNWTs are being emerged as a promising technology for future FETs and dominating over planar MOSFETs in dynamic memories and logic. Si NWs are used as a channel material so it is called SiNWTs. SiNWTs have metal source and drain terminals, like a planar MOSFETs. Thus the contact properties are showing significantly effect on the performance of device. The annealing mechanism is used for formation of ohmic contacts and gradually increasing on-state current and effective mobility. The mean free path of electron is larger than the device length in SiNWTs, thus the carriers scattering events are very less, during the charge transportation within the structure [9].

2.2 GeNWFET

Ge is second most commonly used semiconductor material. It has lower effective mass and higher electron mobility. For long channel MOSFETs, Ge has more drive current and threshold voltage. But in short channel devices, Ge has large external resistance, lack of stressing methods and large variability. So it is not an ideal candidate for channel replacement in short channel devices [10].

3 Device Design

In this work, we have designed three different cross section shapes GAANWT such as triangular, trapezoidal and pentagonal cross sections for parameters as given in Table 1.

Table 1 Design parameters of device

Parameters	Value
Lambda Design Rule	10nm
Structure orientation	<100>
Channel Height	6,8,10,12 (nm)
Channel Diameter	6.5,8,10,12 (nm)
Gate oxide	1nm
Channel length	20nm
Substrate	2e17
Source/drain	2.063e20
Channel	1e15

Fig. 2 shows a 3-D perspective view and 2-D cross section of the channel region of the GAA NWFET. Tungsten W (4.5eV) is used for gate terminal, source, drain, metal contacts, HfO₂ (k = 20-25) is used as gate oxide to isolate the channel from gate. Two different channel materials Si and Ge are used and a comparative analysis has been done for these devices. For metal contacts and electrodes, Aluminum (Al) and Tungsten (W) are used respectively. The device is designed for different heights with a constant channel width 10nm and for different widths taking constant height 10nm respectively. Remaining parameters are common for all devices. The 3D device structure is simulated with Visual TCAD.

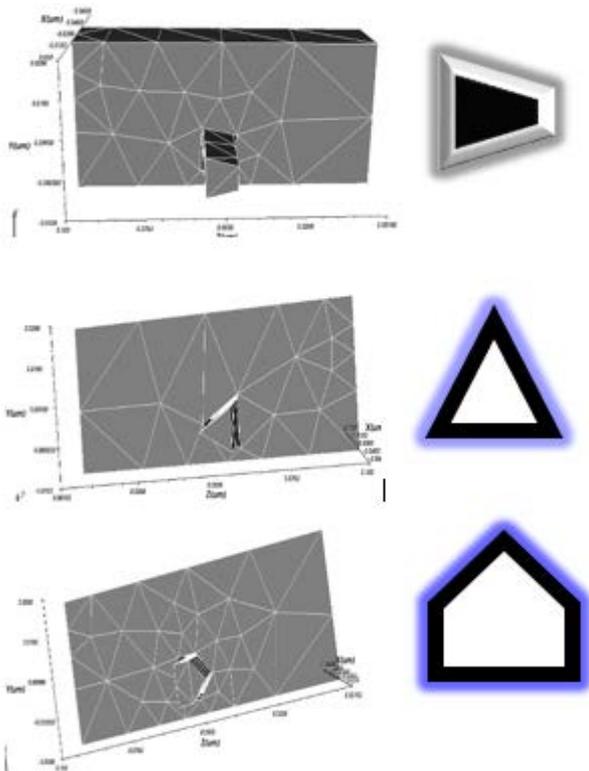
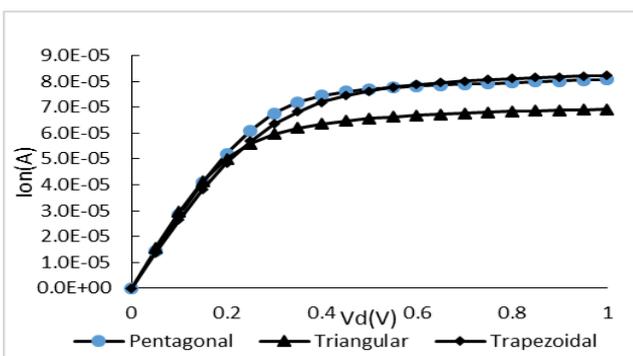


Fig. 2 Schematic Representation of 3-D perspective view and 2-D cross sections.

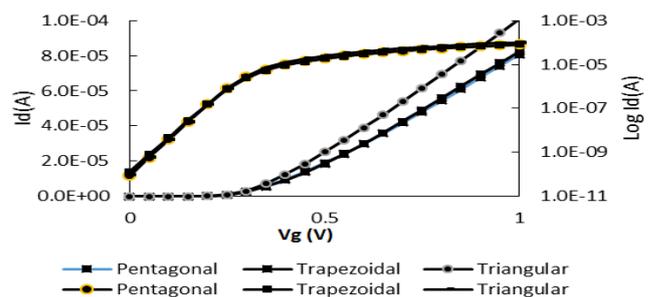
4 Device Simulations and Analysis

The device is simulated with mentioned numerical values, classical drift-diffusion mechanism and 300K constant temperature. All simulations have been done with a range of drain voltage such as $V_d =$

0.05-1V. The Threshold voltage (V_{ti}) for all designed NWTs have been extracted from transfer characteristics in active region with drain voltage $V_d = 0.05V$. I_{off} current is taken at $V_g = 0.00V$ and drive current (I_{on} Current) is taken at $V_g = 1.00V$ with constant drain voltage $V_d = 0.5V$. The DIBL parameter is obtained as the horizontal displacement of I-V characteristics at drain current $1.0e-7$ A and constant drain voltage $V_{lin}=0.05V$ and $V_{sat} = 1.0V$. The subthreshold swing is obtained from transfer characteristics. The output characteristics of GAA NWFET devices have been extracted with varying drain voltage (0-1.0V) on constant gate voltage $V_{gs}=1.0V$. The transfer characteristics of GAA NWFET devices have been extracted with varying gate voltage on constant drain voltage $V_{ds}=1.0V$. Fig. 3 shows the relation of I_d-V_d and I_d-V_g of devices. Fig. 3(a) and (c) depicts that the drain current is directly proportional to the voltage in linear region. It is linearly increasing with drain voltage V_d . Further I_d gets saturated w.r.t. V_d and it is called saturation region. TrNWT has maximum I_{on} current as compared to TNWT and PNWT because I_{on} current is directly proportional to cross section area. Higher cross section area device has more conducting area and more charge carriers. TNWT has minimum cross section area thus it shows the minimum I_{on} current. Fig. 3(b) and (d) show the transfer characteristics of SiNWT and GeNWT with different cross section shapes. I_d-V_g plots show that SiNWT has small V_{ti} than GeNWT.



(a)



(b)

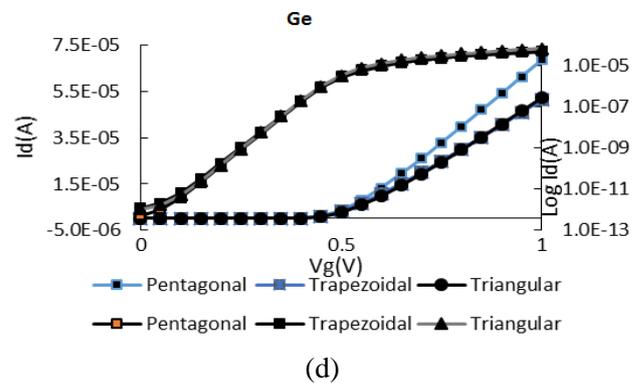
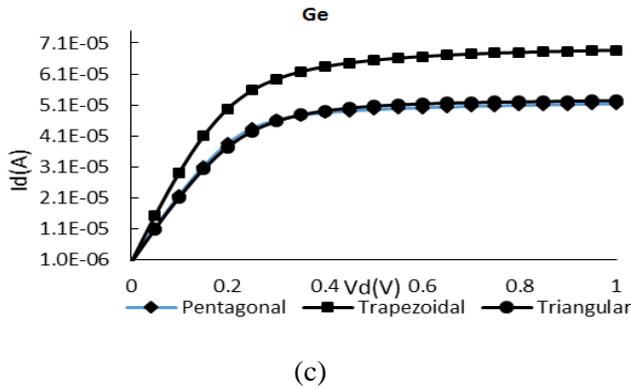


Fig. 3 Characteristics with different cross sectional shapes (a) Output characteristics of SiNWT (b) Transfer characteristics of SiNWT (c) Output characteristics of GeNWT (d) Transfer characteristics of GeNWT

Fig. 4 shows the comparative analysis of electrical characteristics like I_{on} , I_{off} , I_{on}/I_{off} , V_{ti} , SS and DIBL of GAA NWT with different shapes and different channel materials. Fig. 4(a) shows that TrNWT with Si channel has maximum I_{on} Current ($6.5E-05$). Si has higher DoS as compared to Ge, so it shows higher I_{on} current in short channel designed devices. Fig. 4(b) shows the I_{off} current of different devices. I_{off} current is a kind of leakage current which is present in the device when no voltage is applied. Ge channel devices have better leakage current than Si channel devices.

Fig. 4(c) shows the I_{on}/I_{off} ratio of different devices. I_{on}/I_{off} presents the switching speed of devices and it is approximately anti-proportional to the cross section area. TNWT with Ge channel shows the maximum I_{on}/I_{off} ratio ($7.43E07$) as compared to other devices. Fig. 4(d) depicts the SS of GAA NWT devices. The minimum value of SS shows fast switching and lower SCEs. Basically SS depends upon corner effect, channel length and gate control ability. Thus SiPNWT has minimum SS ($62.2mV/dec$) and GeTNWT has maximum SS ($65.3mV/V$). Fig. 4(e) shows the DIBL of GAANWT. DIBL is a kind of SCEs which is inversely proportional to the cross section area. Thus SiPNWT has minimum DIBL ($10mV/V$) and SiTNWT has maximum DIBL ($14mV/V$).

Fig. 4(f) shows the V_{ti} characteristics of GAANWT. Threshold voltage defines the voltage at which the device starts working. It shows the power consumption. Basically short channel devices are used in low power applications and need to have lower threshold voltage. It is found that V_{ti} is anti-proportional to cross section area. So Si TNWT has maximum V_{ti} ($0.2386V$) and TrNWT has minimum V_{ti} ($0.2285V$). V_{ti} ($0.2294V$) of Si PNWT lies in

between TNWT and TrNWT. The same relations are hold by GeNWT. Ge TrNWT has minimum V_{ti} ($0.4217V$).

Table 2 presents the effects of cross sections shapes and channel materials on I_{on} and I_{on}/I_{off} ratio of NWT. Table 3 shows the variation of SCEs with variation of channel materials and shapes. Table 4 presents the comparison between different cross sections and channel materials. It was found that PNWT can improve the electrical results. PNWTs have better performance in terms of SCEs like SS and DIBL and optimum I_{on}/I_{off} ratio, whereas Si Trapezoidal NWTs have shown maximum I_{on} current because of maximum conducting area. But due to losses of gate controllability, it has maximum SCEs.

4.1 Impact of different D and H on transfer and output characteristics

From previous results, it is clear that PNWT has shown the better SCE and I_{on}/I_{off} . TrNWT has shown high I_{on} and high SS. In this section, PNWT and TrNWT have been designed and simulated with different diameters and heights. A comparative study of electrical characteristics with respect to diameters has been done. All simulations are done with gate voltage $V_{gs} = 0 - 1V$, Drain voltage $V_d = 0.5V$, varying Diameter $D = 6.5nm, 8nm, 10nm, 12nm$ with constant height of $10nm$ and varying Height $H = 6nm, 8nm, 10nm, 12nm$ with constant diameter of $10nm$. I_{on} at $V_{gs} = 1V$; I_{off} at $V_{gs} = 0V$ is observed.

Fig. 5 (a-c) shows the electrical characteristics in terms of I_{on} , I_{off} , I_{on}/I_{off} of PNWT with varying Diameters. Fig. 5 (d-f) shows the variation of I_{on} , I_{off} and I_{on}/I_{off} ratio with varying height in PNWT. Here

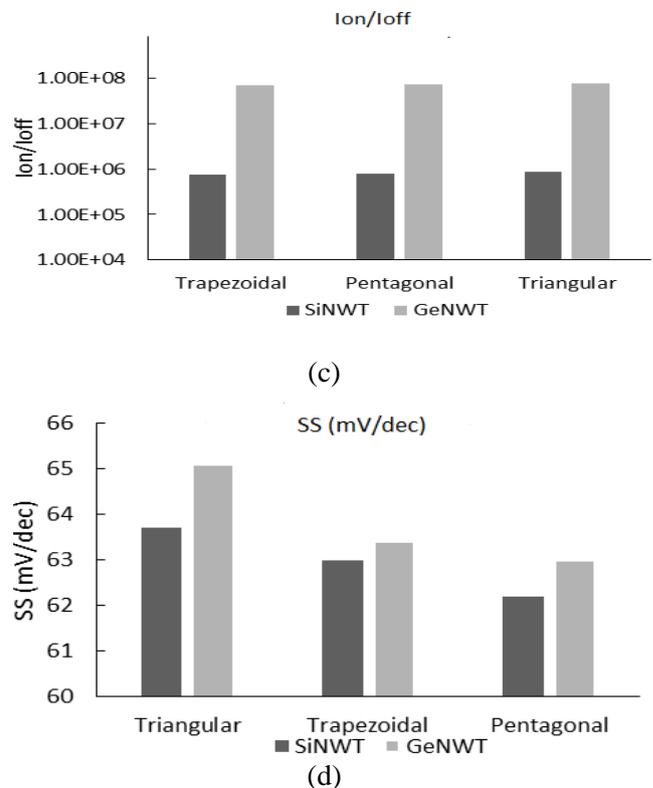
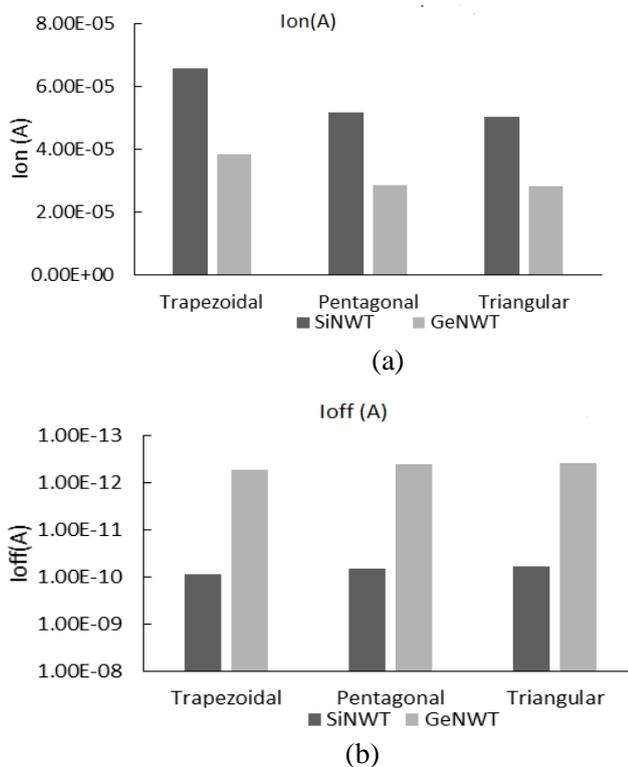
It is found that I_{on} increased with diameter due to increment of cross section area. Here cross section area is more dominating factor to increase the I_{on} current. Ge PNWT with 12nm diameter has maximum I_{on} current and I_{on}/I_{off} ratio, but with 6.5nm diameter, PNWT has minimum I_{on} current. Same relation is justified for different heights. I_{on} is increased with increasing of height due to increment in cross section area. Fig. 5 (g-i) shows the I_{on} , I_{off} , I_{on}/I_{off} of TrNWT with varying diameters respectively. Fig. 5 (j-l) shows the variation of I_{on} , I_{off} and I_{on}/I_{off} ratio with varying height in TrNWT. TrNWT has larger cross section area than PNWT. So it has larger I_{on} current. I_{on} increased with increase in diameter and height. Tr NWT with 12nm has maximum I_{on} and 6.5nm TrNWT has minimum I_{on} current and I_{on}/I_{off} ratio. Table 5 and Table 6 show the simulated results of PNWT and TrNWT with different height, diameter and different channel materials respectively.

4.2 SCEs with varying D and H

Subthreshold swing depends on gate controllability. So for lower diameter device, gate controllability is higher than larger diameter devices. SS is measured at $V_d = 0.5V$, diameter $D = 6.5nm, 8nm, 10nm, 12nm$ with constant height of 10nm and height $H = 6nm, 8nm, 10nm, 12nm$ with constant diameter of

10nm. Fig. 6 show the comparative analysis of SS of PNWT and TrNWT with different D, H and channel materials. Fig. 6(a) and (b) show the SS of PNWT with D and H respectively. Fig. 6(c) and (d) show the SS of TrNWT with varying of D and H respectively. PNWT and TrNWT with 6.5nm diameter have minimum SS and both the devices with 12 nm diameter has maximum SS. The same relation has proved true for height. But Si channel devices have better performance in terms of SCEs than Ge.

DIBL is also a kind of SCEs and it depends on the gate controllability and the gate length. But for lower diameter device, gate controllability is higher than larger diameter devices. DIBL is measured at $V_{ds,sat} = 1.0V$ and $V_{ds,lin} = 0.05V$, varying diameter $D = 6.5nm, 8nm, 10nm, 12nm$ with constant height of 10nm, varying height $H = 6nm, 8nm, 10nm, 12nm$ with constant diameter of 10nm. Fig. 7 shows the DIBL of PNWT and TrNWT with different D, H and channel materials. The minimum diameter has small cross section area and better gate controlling. So PNWT and TrNWT with 6.5nm diameter show the minimum DIBL, and with 12 nm, show the maximum DIBL. Table 7 and Table 8 show the simulated SS and DIBL results of PNWT and TrNWT with different height, diameter and different channel materials respectively.



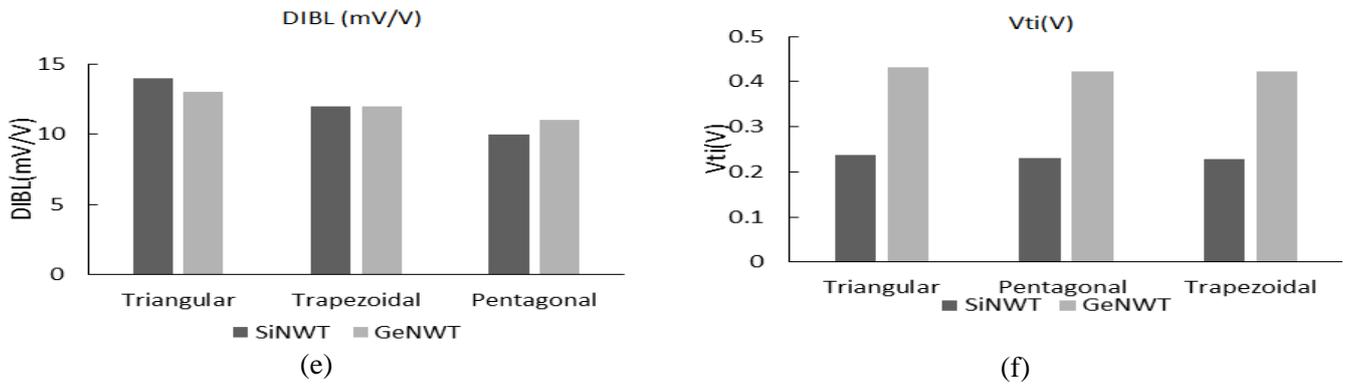
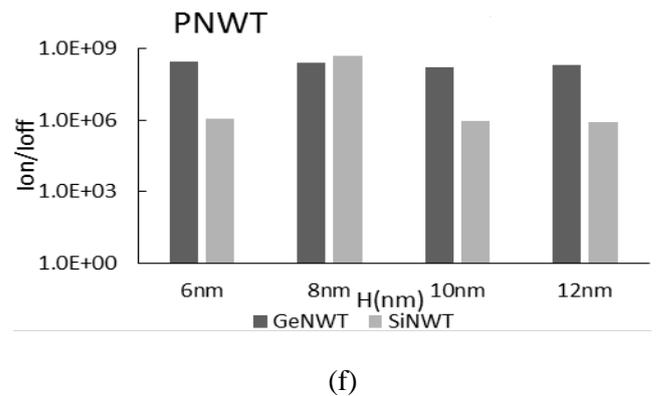
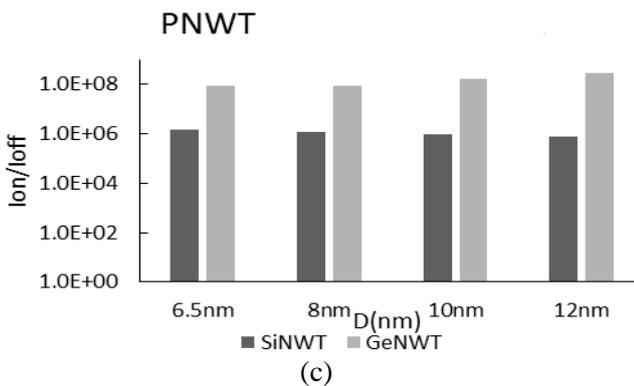
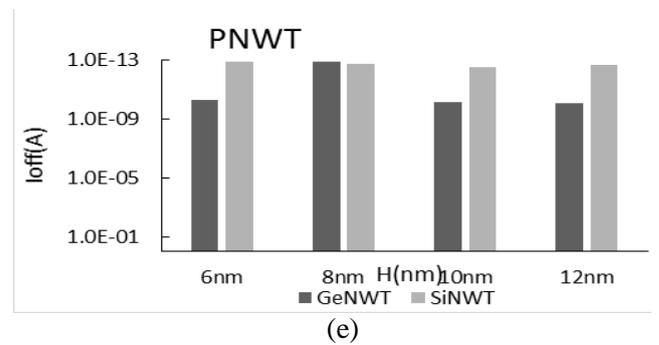
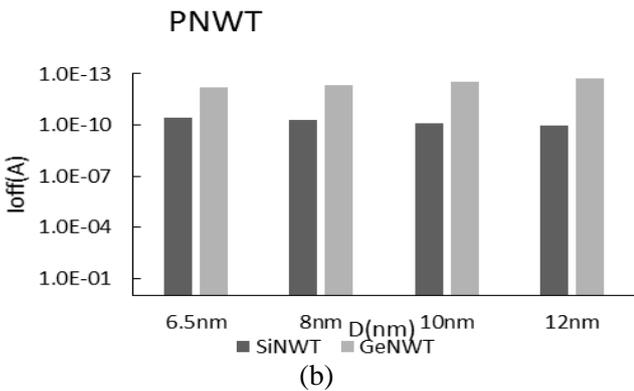
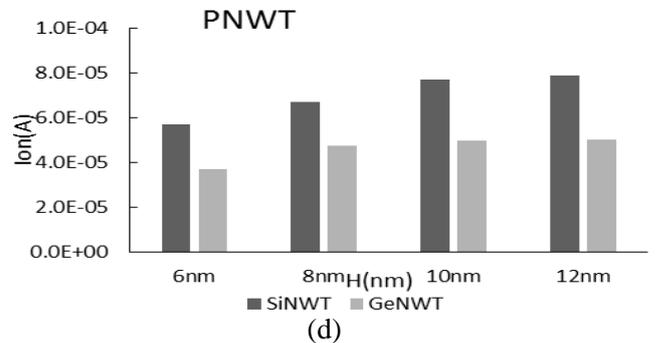
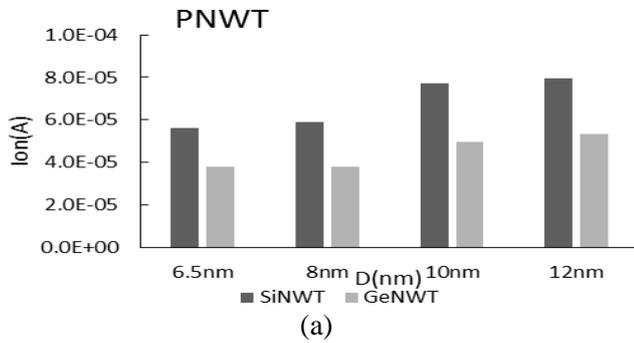


Fig. 4 Comparative analysis of (a) On current of SiNWT and GeNWT, (b) Off current of SiNWT and GeNWT (c) I_{on}/I_{off} ratio of SiNWT and GeNWT.(d) SS of SiNWT and GeNWT, (e) DIBL of SiNWT and GeNWT and (f) V_{ti} of SiNWT and GeNWT.



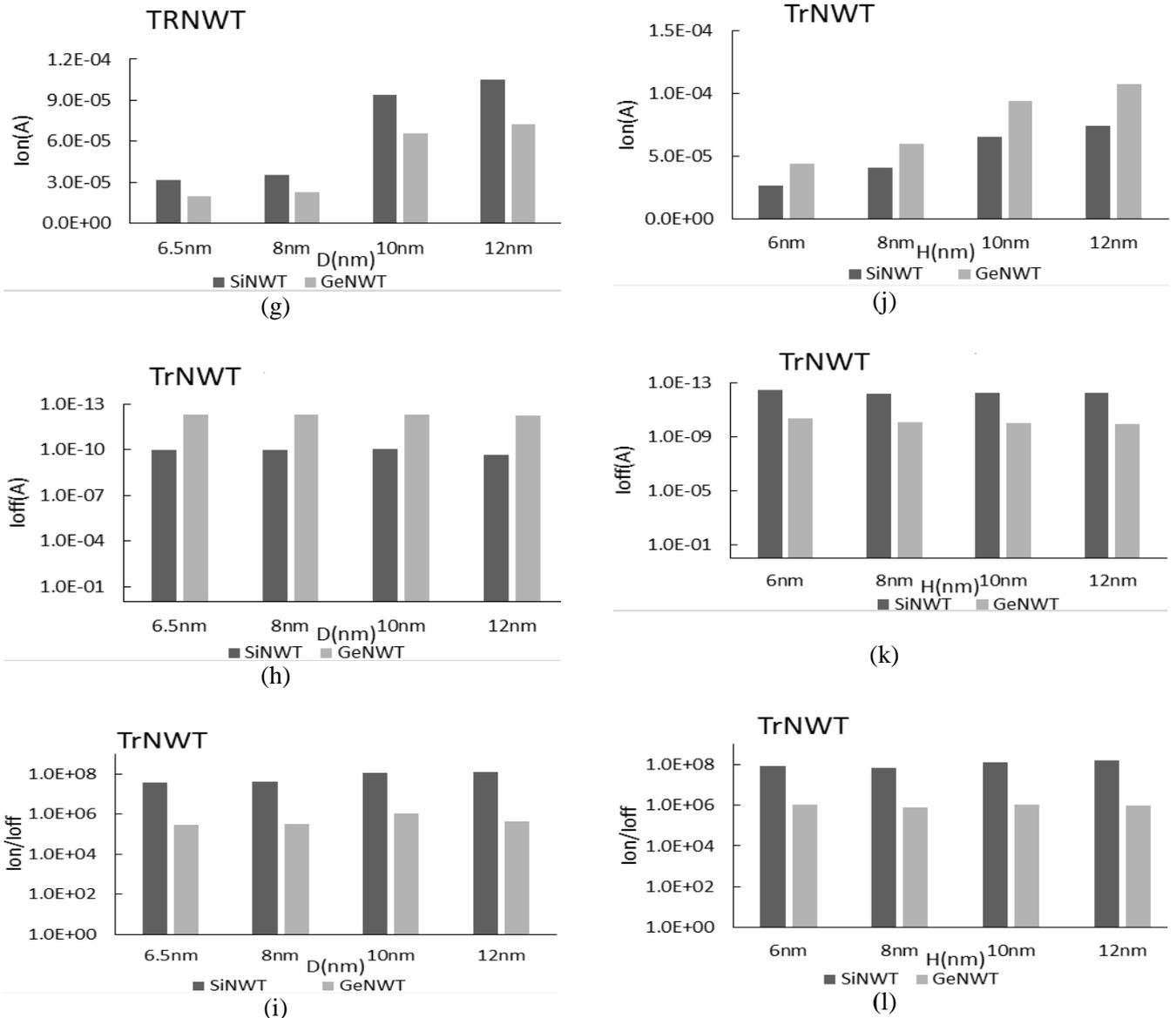
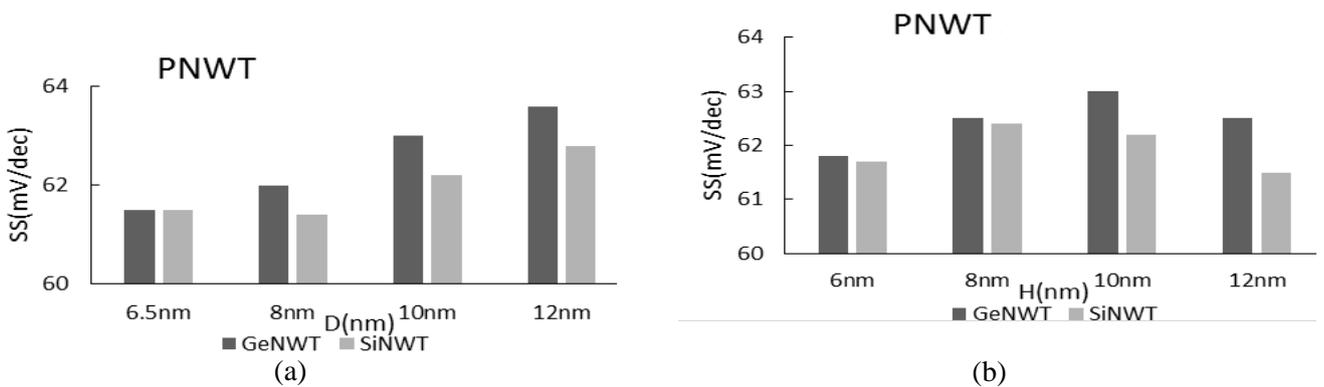


Fig. 5 (a) I_{on} of PNWT w.r.t. D , (b) I_{off} of PNWT w.r.t. D , (c) I_{on}/I_{off} ratio of PNWT w.r.t. D , (d) I_{on} of PNWT w.r.t. H , (e) I_{off} current of PNWT w.r.t. H (f) I_{on}/I_{off} ratio w.r.t. H , (g) I_{on} of TrNWT w.r.t. D , (h) I_{off} of TrNWT w.r.t. D , (i) I_{on}/I_{off} ratio w.r.t. D , (j) I_{on} of TrNWT w.r.t. H , (k) I_{off} w.r.t. H , (l) I_{on}/I_{off} ratio w.r.t. H for Si and Ge channel materials.



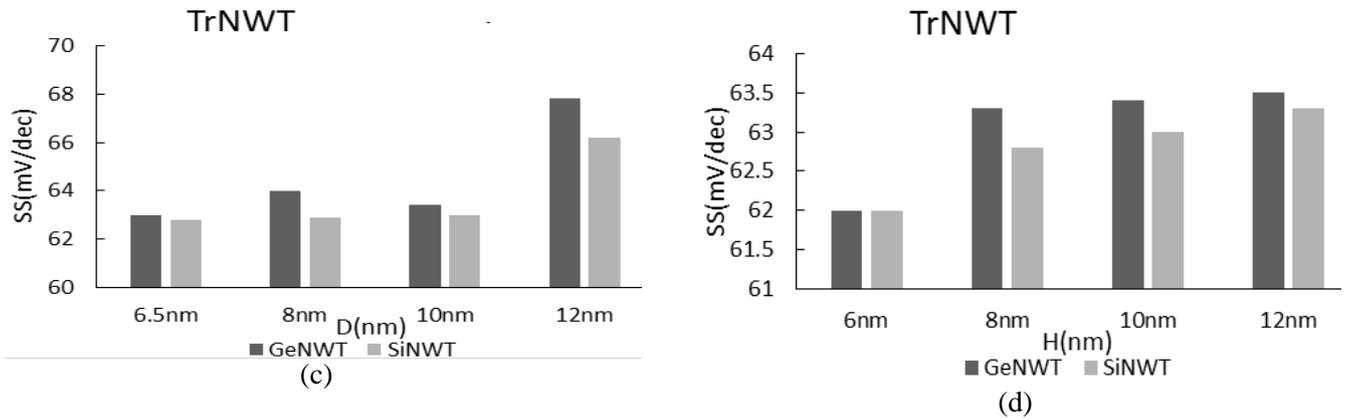


Fig. 6 Comparative analysis (a) SS of PNWT w.r.t. D, (b) SS of PNWT with w.r.t. H, (c) SS of TrNWT w.r.t. D and (d) SS of TrNWT w.r.t. H with Ge and Si channel materials.

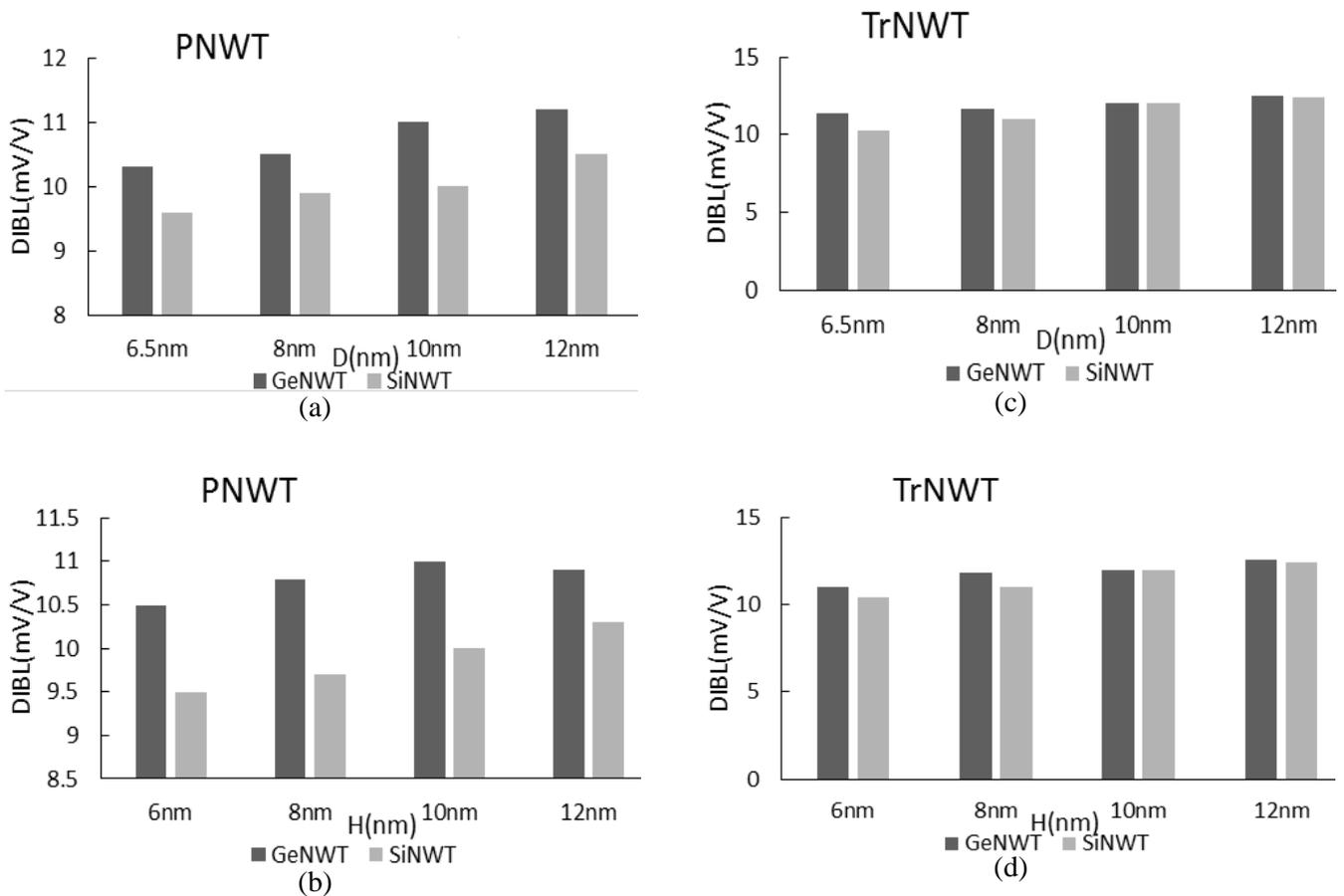


Fig. 7 Comparative analysis of (a) DIBL of PNWT with varying D, (b) DIBL of PNWT with varying H, (c) DIBL of TrNWT with D and (d) DIBL of TrNWT with varying H with Ge and Si channel materials.

Table 2 Simulated results of GAANWT with different cross section shapes and channel materials

Cross Section Shape	$I_{on}(A)$		$I_{off}(A)$		I_{on}/I_{off}	
	Si	Ge	Si	Ge	Si	Ge
TNWT	5.05E-05	2.84E-05	5.9E-11	3.82E-13	8.54E05	7.43E07
PNWT	5.18E-05	2.88E-05	6.5E-11	4.02E-13	7.89E05	7.16E07
TrNWT	6.57E-05	3.83E-05	8.8E-11	5.47E-13	7.44E05	7.00E07

Table 3 Simulated results of SCEs for GAANWT with different cross section shapes and channel materials

Cross Section Shape	SS (mV/dec)		DIBL(mV/V)		$V_{ti}(V)$	
	Si	Ge	Si	Ge	Si	Ge
TNWT	63.7	65.1	14	13	0.2366	0.4317
PNWT	63	63.4	12	12	0.2294	0.4228
TrNWT	62.2	63	10	11	0.2285	0.4217

Table 4 Simulated results of GAANWT with different cross section shapes and channel materials

		PNWT vs TNWT / TrNWT	Triangular [5]
I_{on}	Si	+2.89 % than TNWT 21% less than TrNWT	+5 times
	Ge	+1.40% than TNWT 24% less than TrNWT	+3 times
I_{on}/I_{off}	Si	7.50% less than TNWT +6.04% than TrNWT	-4 times
	Ge	3.63% less than TNWT +2.28% than TrNWT	17 times
SS	Si	2.35% less than TNWT 1.26% less than TrNWT	-0.49%
	Ge	3.22% less than TNWT 0.63% less than TrNWT	-1.56%
DIBL	Si	28% less than TNWT 16% less than TrNWT	same
	Ge	15% less than TNWT 8.33% less than TrNWT	-21%
V_{ti}	Si	3.04% less than TNWT +0.39% than TrNWT	-26%
	Ge	2.06% less than TNWT +0.26% than TrNWT	+36.38%

Table 5 Simulated results of PNWT with different height, diameter and channel materials

	PNWT	6.5/6nm		8nm		10nm		12nm	
		Ge	Si	Ge	Si	Ge	Si	Ge	Si
D	I_{on} (A)	3.80E-5	5.62E-5	3.86E-5	5.92E-5	4.95E-5	7.60E-5	5.323E-5	7.90E-5
	I_{off} (A)	6.61E-5	3.69E-11	4.27E-13	4.98E-11	2.98E-13	7.94E-11	1.76E-13	1.06E-10
	I_{on}/I_{off}	8.90E7	1.56E6	8.90E7	1.18E6	1.66E8	9.68E5	3.02E8	7.48E5
H	I_{on} (A)	3.70E-5	5.68E-5	4.73E-5	6.71E-5	4.95E-5	7.69E-5	5.02E-5	7.90E-5
	I_{off} (A)	1.25E-13	4.58E-11	1.88E-13	1.29E-13	2.98E-13	7.94E-11	2.33E-13	9.33E-11
	I_{on}/I_{off}	2.96E8	1.17E6	2.50E8	5.20E8	1.66E8	9.68E5	2.14E8	8.47E5

Table 6 Simulated results of TrNWT with different height, diameter and channel materials

	TrNWT	6.5/6nm		8nm		10nm		12nm	
		Ge	Si	Ge	Si	Ge	Si	Ge	Si
D	I_{on} (A)	2.01E-5	3.15E-5	2.30E-5	3.54E-5	6.54E-5	9.40E-5	7.24E-5	10.49E-5
	I_{off} (A)	5.21E-13	1.06E-10	5.41E-13	1.13E-10	5.47E-13	8.82E-11	5.75E-13	2.40E-10
	I_{on}/I_{off}	3.86E7	2.97E5	4.24E7	3.13E5	1.19E8	1.06E6	1.25E8	4.37E5
H	I_{on} (A)	2.66E-5	4.38E-5	4.04E-5	5.97E-5	6.54E-5	9.40E-5	7.42E-5	10.79E-5
	I_{off} (A)	3.42E-13	4.17E-11	6.14E-13	7.40E-11	5.47E-13	8.82E-11	4.90E-13	1.10E-10
	I_{on}/I_{off}	7.77E7	1.05E6	6.58E7	8.06E5	1.19E8	1.06E6	1.51E8	9.79E5

Table 7 Simulated SS results of PNWT with different D, H and channel materials

	PNWT	6.5/6nm		8nm		10nm		12nm	
		Ge	Si	Ge	Si	Ge	Si	Ge	Si
D	SS (mV/dec)	65.5	61.5	62	61.4	63	62.2	63.6	62.8
	DIBL (mV/V)	10.3	9.6	10.5	9.9	11	10	11.2	10.5
H	SS (mV/dec)	61.8	61.7	62.5	62.4	63	62.2	62.5	61.5
	DIBL (mV/V)	10.5	9.5	10.8	9.7	11	10	10.9	10.3

Table 8 Simulated SS results of PNWT with different D, H and channel materials

	TrNWT	6.5/6nm		8nm		10nm		12nm	
		Ge	Si	Ge	Si	Ge	Si	Ge	Si
D	SS (mV/dec)	63	62.8	64	62.9	63.4	63.0	67.8	66.2

	DIBL (mV/V)	11.4	10.3	11.7	11	12	12	12.5	12.4
H	SS (mV/dec)	62	62	63.3	62.8	63.4	63	63.5	63.3
	DIBL (mV/V)	11	10.4	11.8	11	12	12	12.6	12.4

5. Conclusion

GAA NWT with different channel materials (Ge and Si) and different cross section shapes like Triangular, Trapezoidal and pentagonal were designed and analyzed for 20nm gate length. The performance of all these GAA structures has been analyzed from output characteristics, transfer characteristics. I_{on} current, I_{on}/I_{off} ratio and SCEs like SS and DIBL have been extracted. It was found that PNWT can improve the electrical results. PNWTs have better performance in terms of SCEs like SS and DIBL and optimum I_{on}/I_{off} ratio, whereas Si Trapezoidal NWTs have shown maximum I_{on} current because of maximum conducting area. But due to losses of gate controllability, it has maximum SCEs. Triangular NWT has good controllability due to the less corner effects so it has less SCEs than TrNWTs but due to small cross section area it has minimum I_{on} current. In this work, Silicon NWTs have better I_{on} and better SCEs than Ge. But Ge has shown better I_{on}/I_{off} ratio and better performance in terms of leakage current. The electrical characteristics with different height and diameter have been analyzed. Pentagonal SiNWT with 6.5nm diameter has minimum SS (61.5 mV/dec) that is very close to ideal value of SS (60mV/dec) and very small DIBL (9.6 mV/V).

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